

# LCFC Confidential

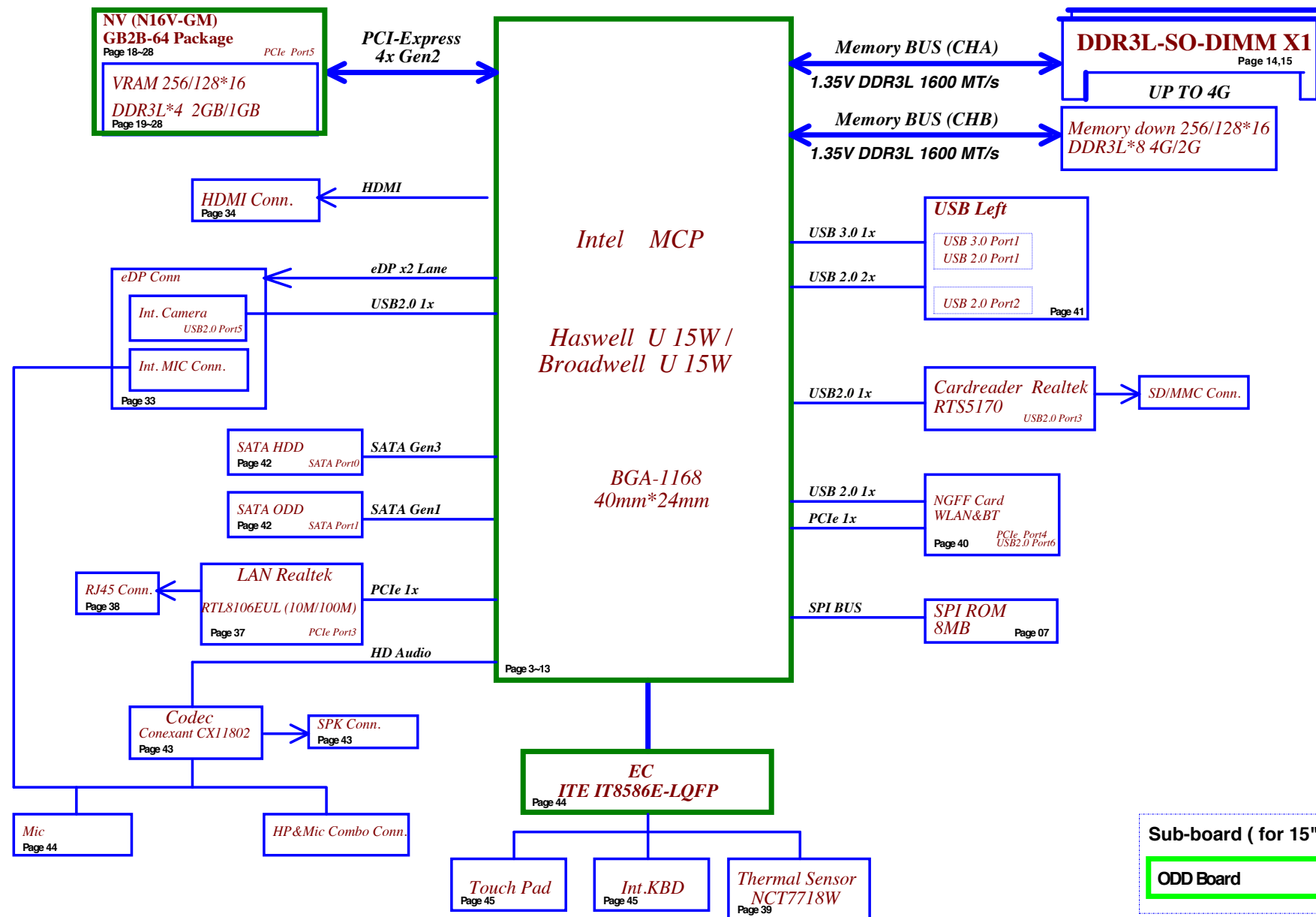
## CG510 M/B Schematics Document

Intel Broadwell U-Processor with DDRIIL + NV920

2015-05-09

REV:0.2

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Issued Date		2015/02/27	Deciphered Date		2013/08/05
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Voltage Rails ( O --> Means ON , X --> Means OFF )

Power Plane / State	B+	+3VALW +5VALW	+3VALW_PCH	+1.35V	+5VS +3VS +1.5VS +1.35VS +1.05VS +0.675VS CPU_CORE  +VGA_CORE +3VGS +1.8VGS +1.35VGS +0.95VGS
S0	O	O	O	O	O
S3	O	O	O	O	X
S3 Battery only	O	O	O	O	X
S5 S4/AC Only	O	O	O	X	X
S5 S4 Battery only	O	X	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB Port Table

USB 2.0 XHCI		USB 3.0 XHCI	
0	USB Port (Right Side)		
1	USB Port1 (Left Side)	1	USB Port1 (Left Side)
2	USB Port2 (Left Side)	2	
3	Cardreader	3	
4	TOUCH PANEL	4	
5	Camera		
6	NGFF(WLAN)		
7			

BOM Structure Table

BOM Structure	BTO Item
@	Not stuff
14@	For 14" part
15@	For 15" part
UMA@	UMA SKU part
PX@	Discrete GPU SKU part
100M@	100M LAN Part
GIGA@	GIGA LAN Part
JET@	For AMD Jet GPU part
TOPAZ@	For AMD Topaz GPU part
RANKA@	For VRAM RankA part
RANKB@	For VRAM RankB part
ME@	ME part(connector, hole)
TS@	For support touch panel sku part
AOAC@	AOAC support part
H2@	Hynix 128Mx16 VRAM part
H4@	Hynix 256Mx16 VRAM part
M2@	Micron 128Mx16 VRAM part
M4@	Micron 256Mx16 VRAM part
S2@	Samsung 128Mx16 VRAM part
S4@	Samsung 256Mx16 VRAM part
H2GX4@	Hynix 128Mx16 VRAM x4pcs sku
M2GX4@	Micron 128Mx16 VRAM x4pcs sku
S2GX4@	Samsung 128Mx16 VRAM x4pcs sku
H4GX4@	Hynix 256Mx16 VRAM x4pcs sku
M4GX4@	Micron 256Mx16 VRAM x4pcs sku
S4GX4@	Samsung 256Mx16 VRAM x4pcs sku
H2GX8@	Hynix 128Mx16 VRAM x8pcs sku
M2GX8@	Micron 128Mx16 VRAM x8pcs sku
S2GX8@	Samsung 128Mx16 VRAM x8pcs sku
H4GX8@	Hynix 256Mx16 VRAM x8pcs sku
M4GX8@	Micron 256Mx16 VRAM x8pcs sku
S4GX8@	Samsung 256Mx16 VRAM x8pcs sku
CDE@	Cost down part
BCDE@	Cost down part for BDW project
SINGLE@	Single Rank VRAM sku
DUAL@	Dual Rank VRAM sku

PCIE PORT LIST

Port	Device
1	
2	
3	LAN
4	WLAN
5	Discrete GPU
6	

SMBUS Control Table

	SOURCE	VGA	BATT	IT8586E	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	TP Module	charger
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VALW	X	V	V +3VALW	X	X	X	X	X	V
EC_SMB_CK2 EC_SMB_DA2	IT8586E +3VS	V +3VGS	X	V +3VS	X	X	V +3VS	X +3VALW_PCH	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	X	V +3VS	V +3VS	X	V +3VALW_PCH	X	X

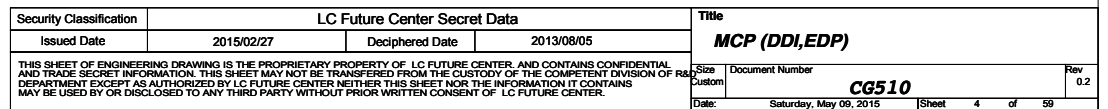
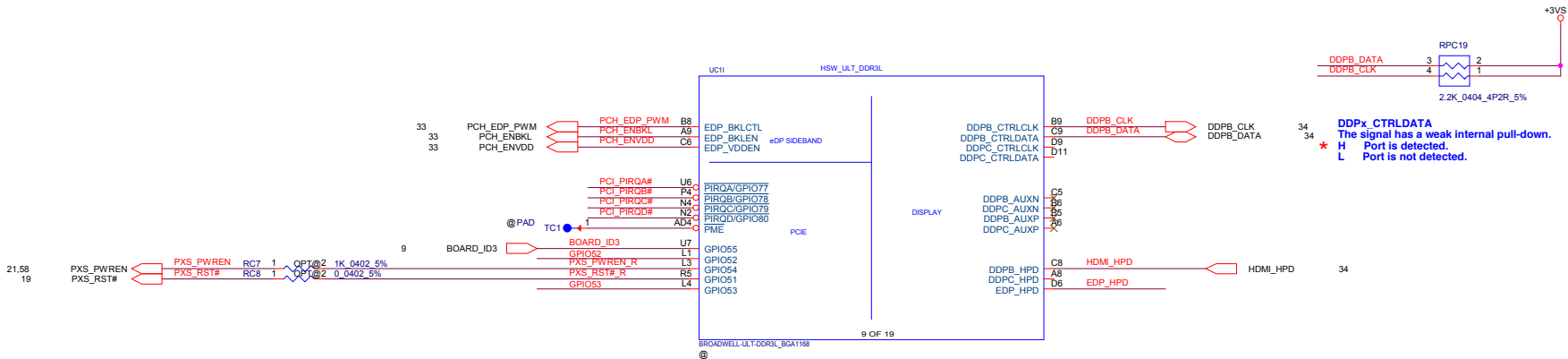
EC SM Bus1 address

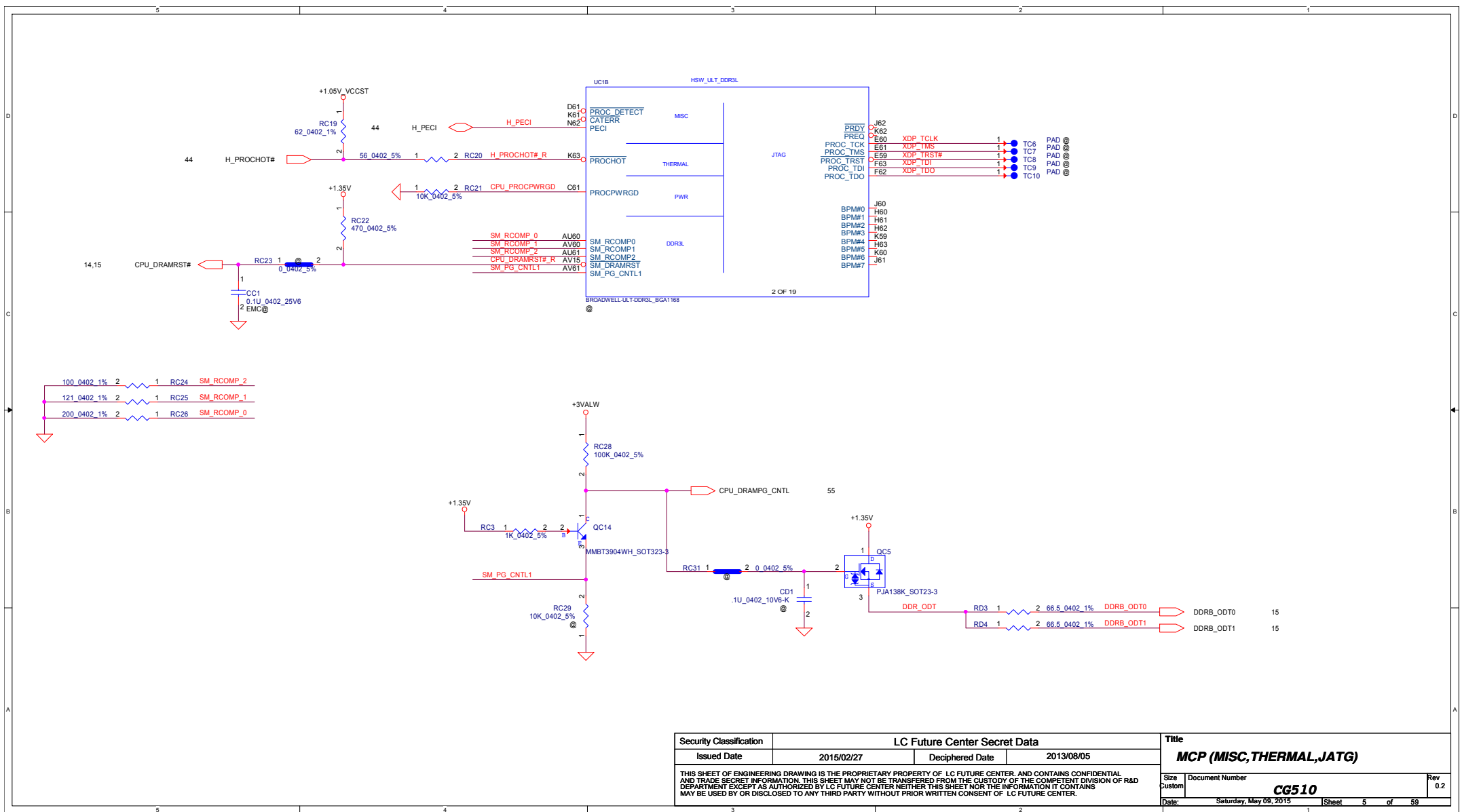
EC SM Bus2 address

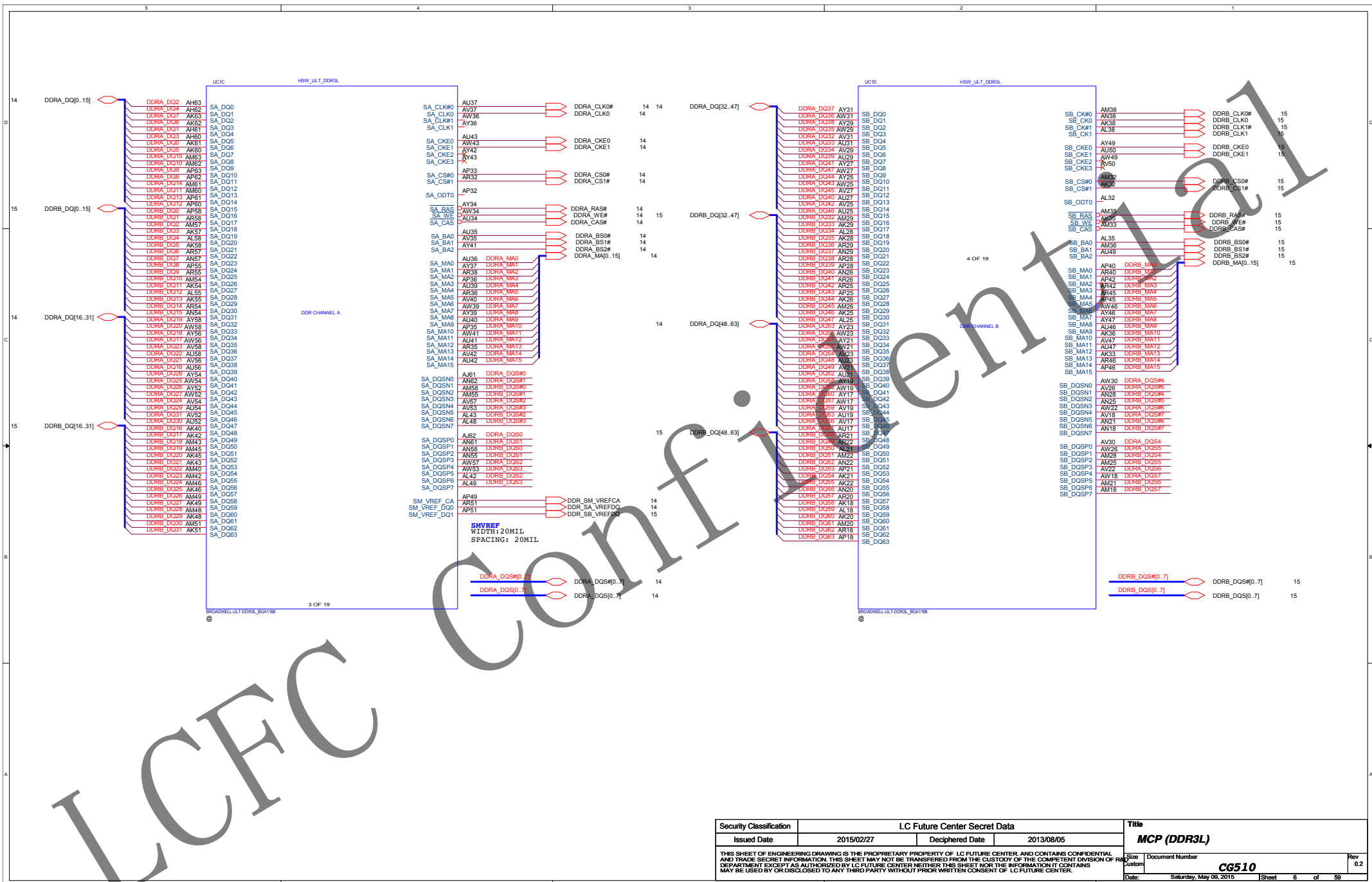
PCH SM Bus address

Device	Address	Device	Address	Device	Address
Smart Battery	0X16	Thermal Sensor NCT7718W	1001_100xb	DDR DIMMA	1010 000Xb
Charger	0001 0010 b	VGA	0x41(default)	DDR DIMMB	1010 010Xb
		PCH	need to update	Wlan	Rsvd

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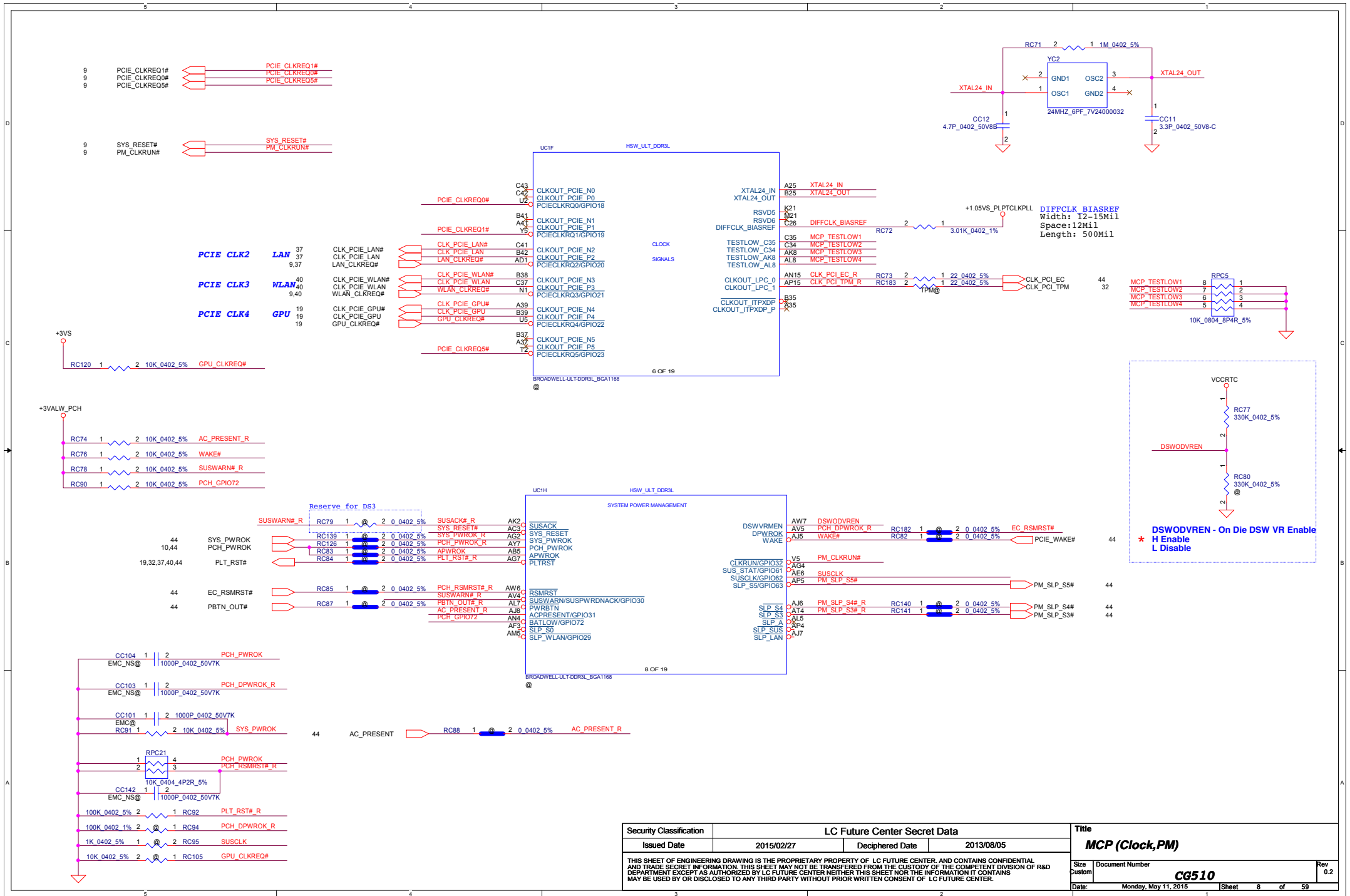






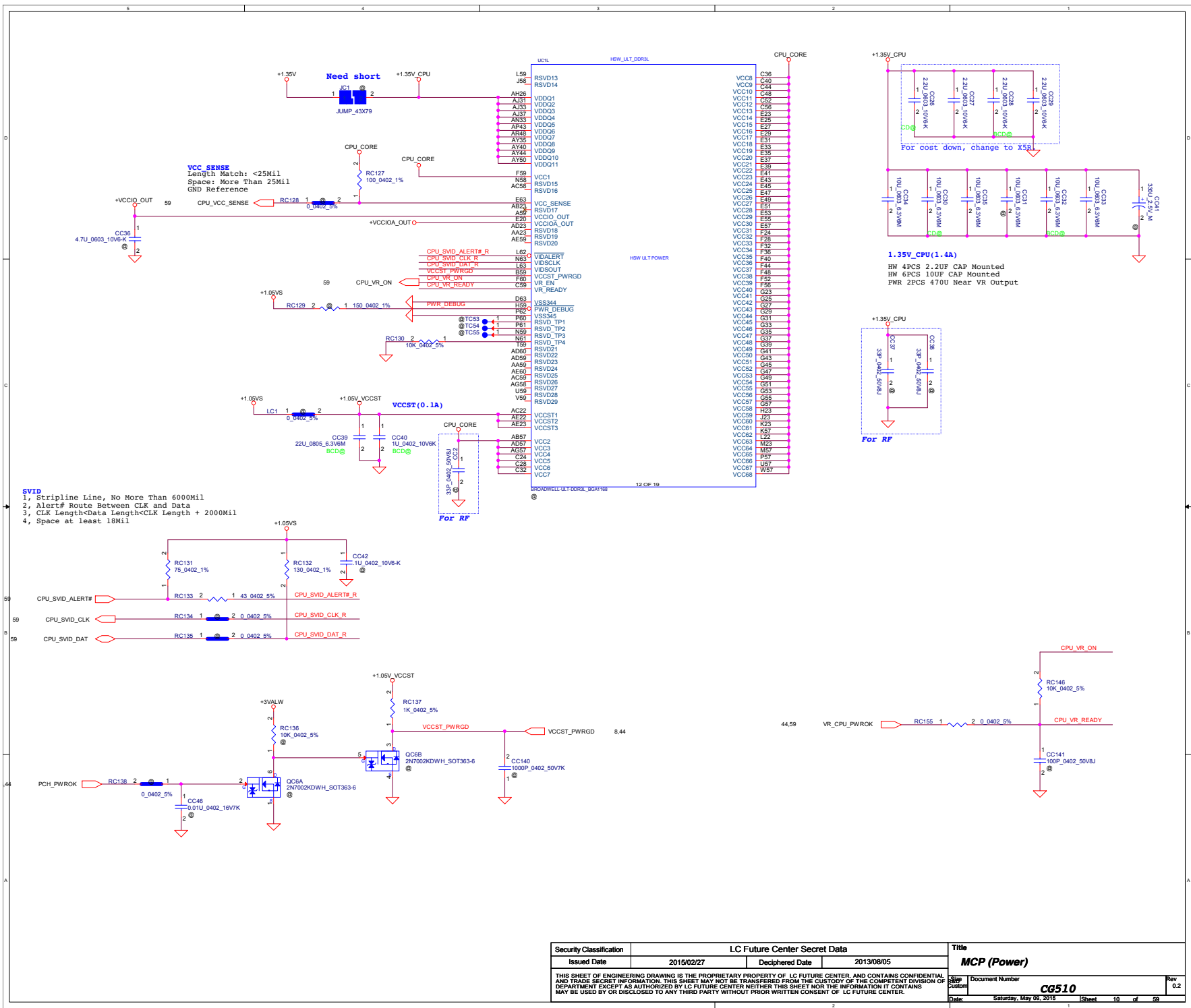
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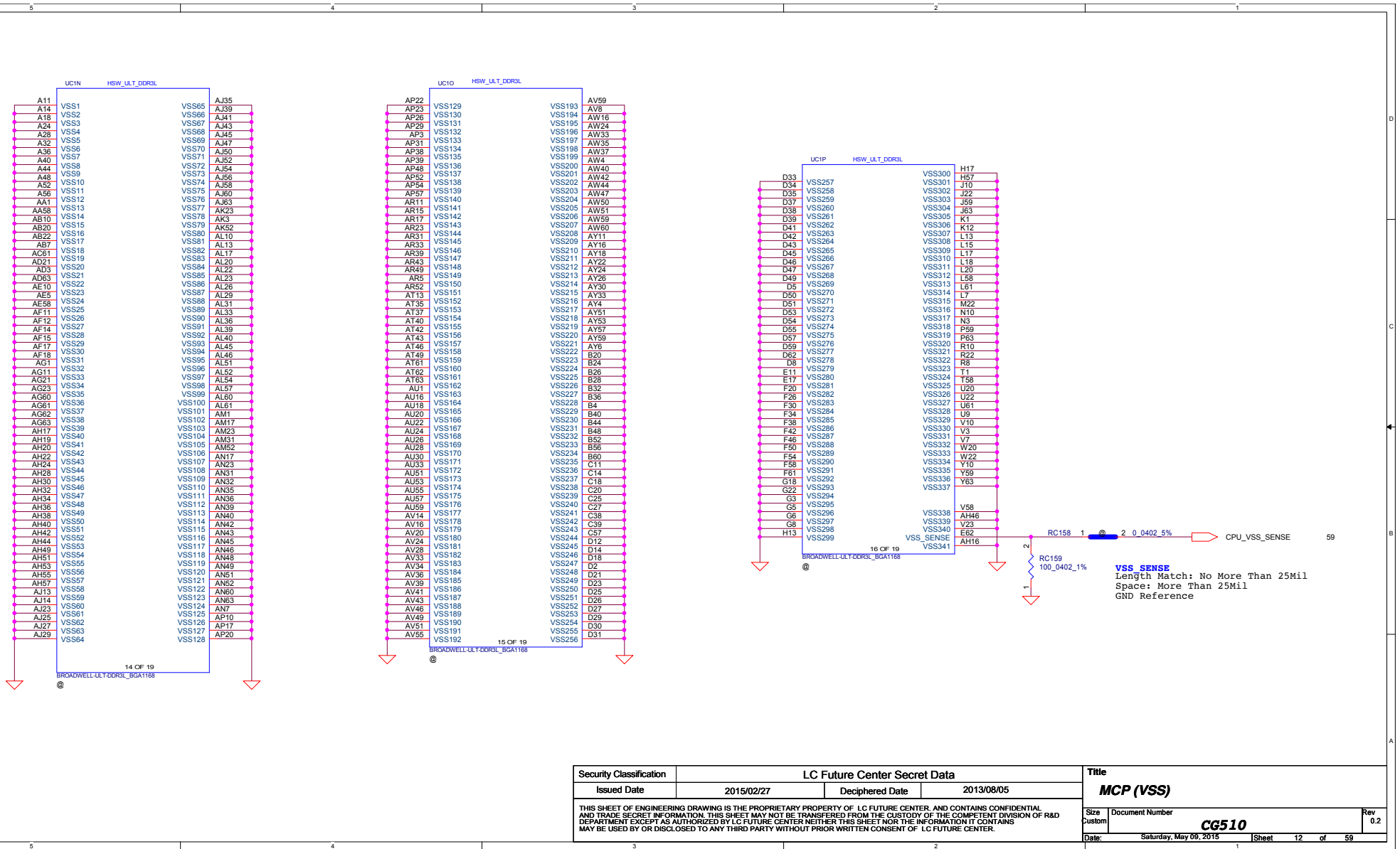


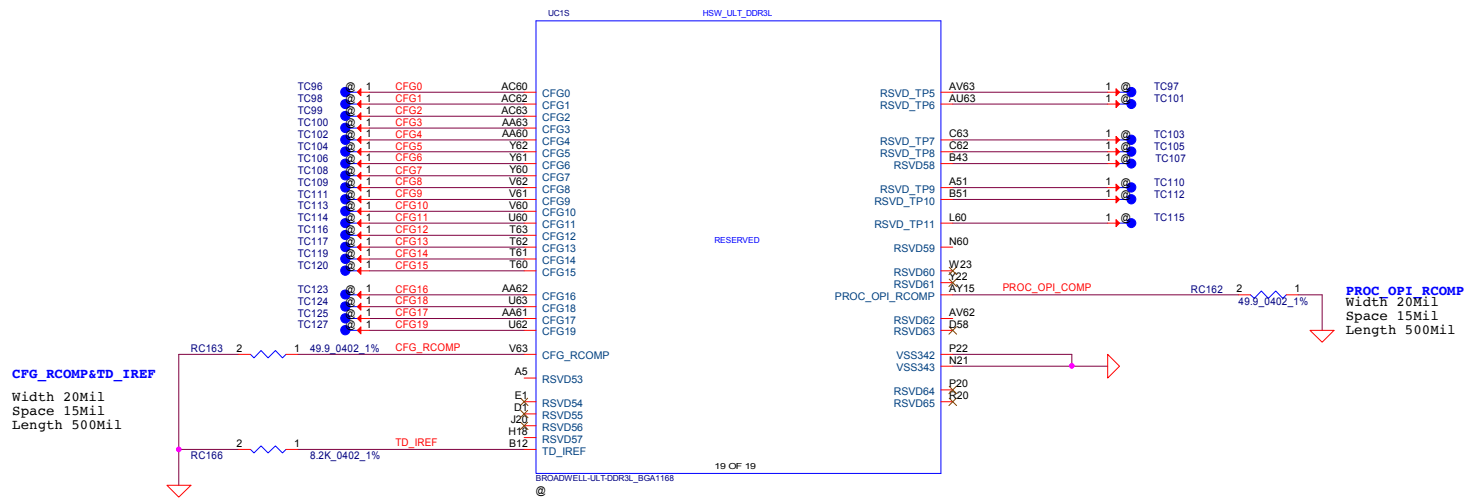
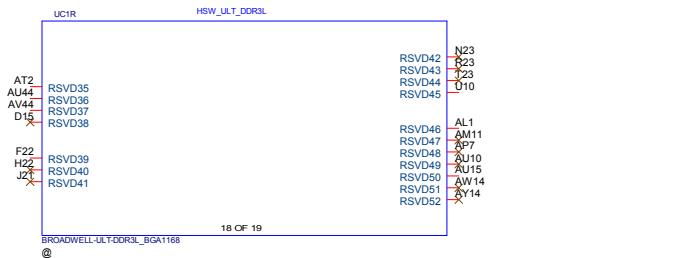
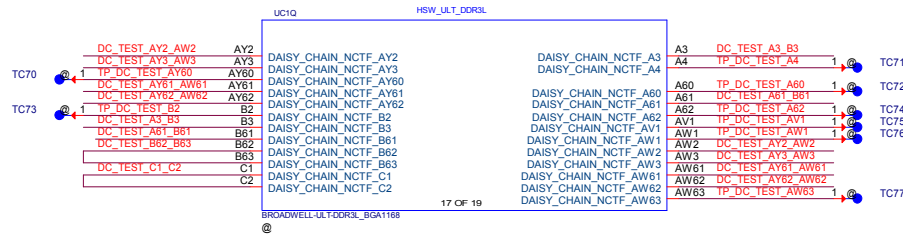










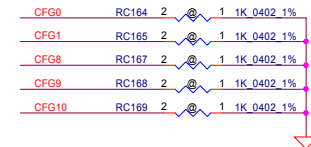


CFG3

\*1: Disable  
0: Enable, Set DFX Enabled BIT  
In Debug Interface MSR

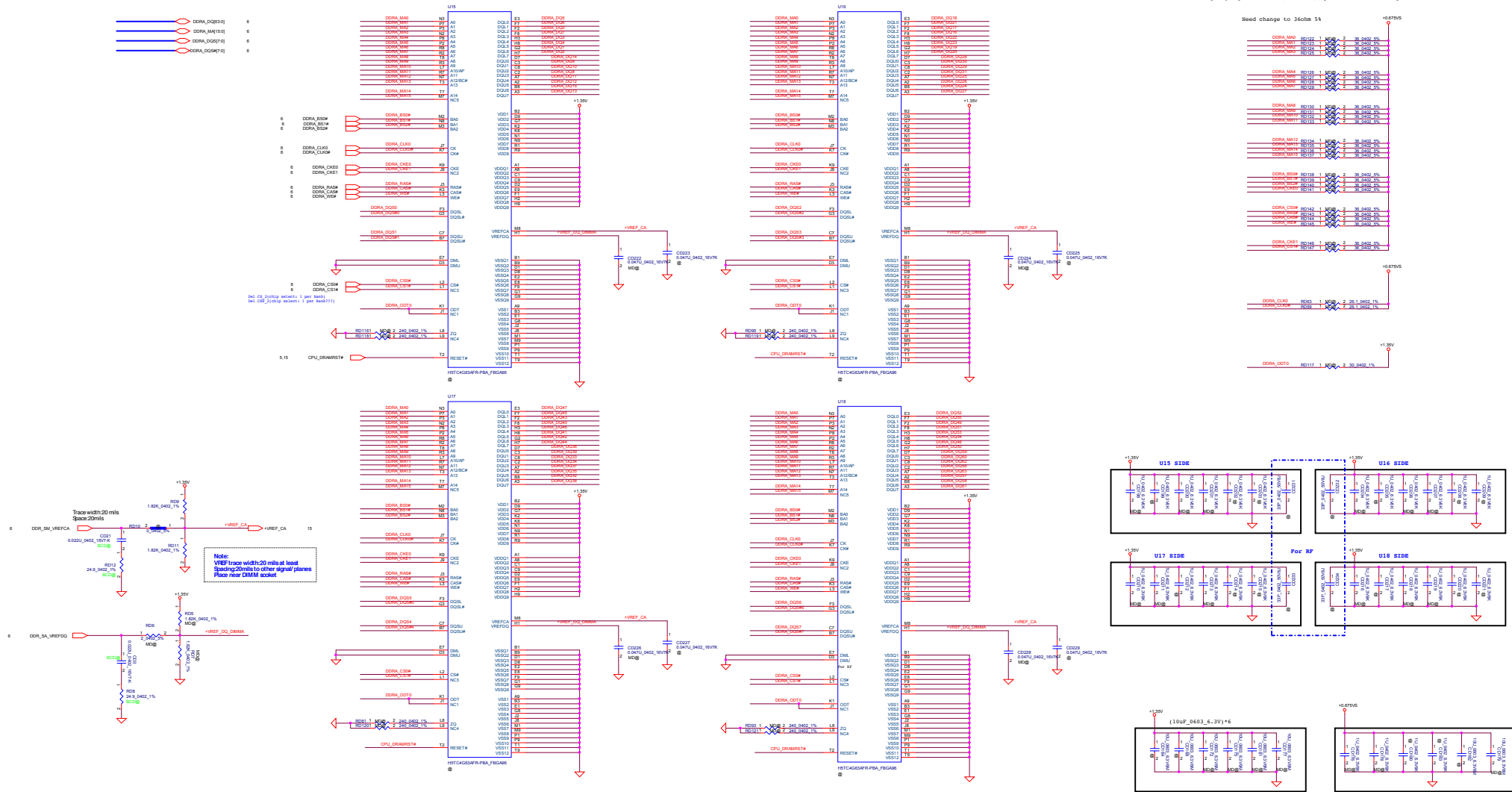
CFG4

\*L: eDP enable  
H: eDP disable

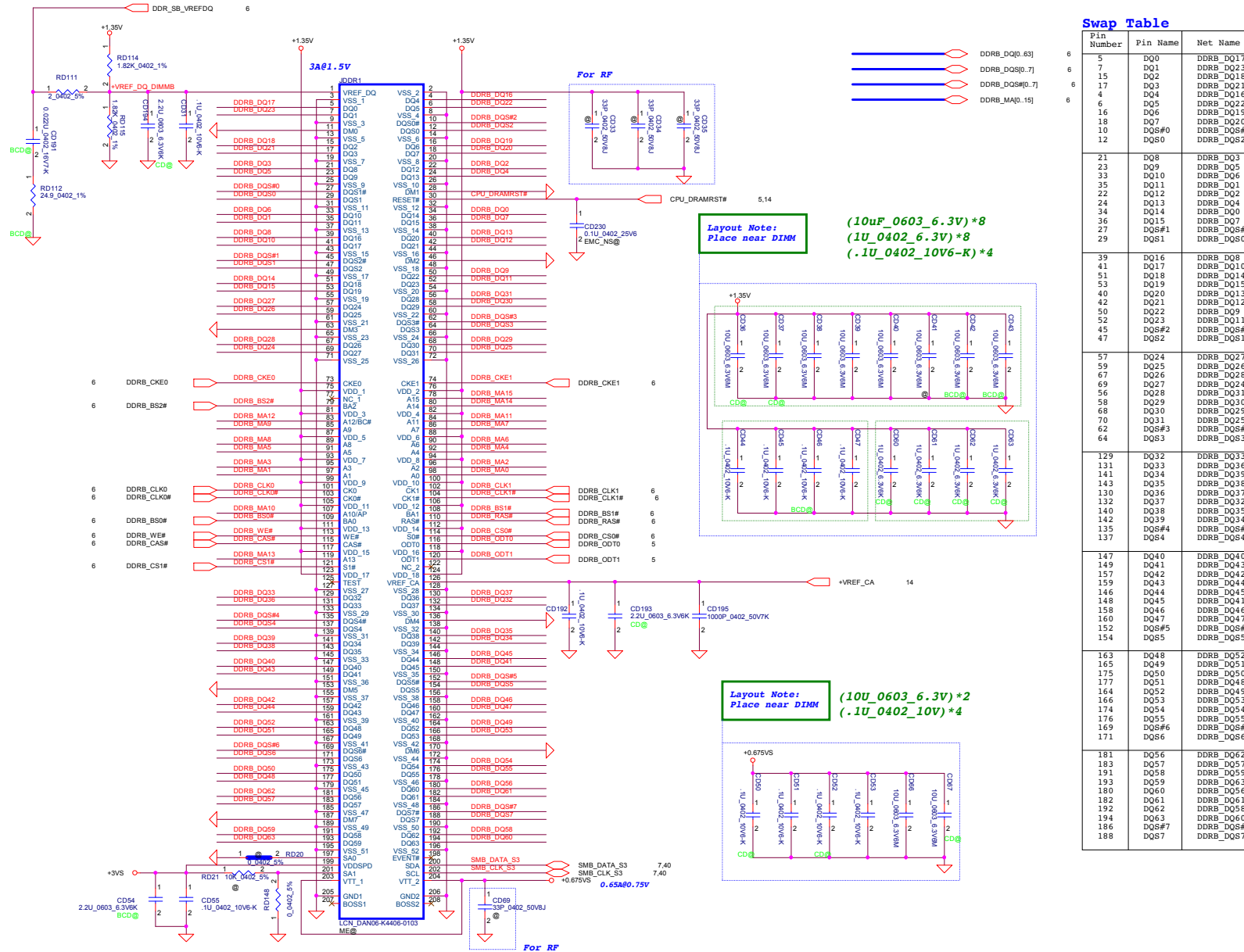


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Signal voltage level = 0.675 V  
 PLACE TWO 4.7K RESISTORS CLOSE TO  
 D1868 OR D1869. VREF\_CA = 0.675V. VREF\_DQ  
 Decoupling caps are needed: One 0.1uF placed close to VREF pins



# DDR3 SO-DIMM B



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N15x GPIO

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	FB Enable for GC6 2.0
GPIO1	OUT	N/A	
GPIO2	OUT	N/A	
GPIO3	OUT	N/A	
GPIO4	OUT	N/A	
GPIO5	OUT	N/A	GPU power sequencing---3V3_MAIN_EN
GPIO6	IN	-	GPU wake signal for GC6 2.0
GPIO7	OUT	N/A	
GPIO8	I/O	-	System side PCIe reset Monitor
GPIO9	I/O	N/A	2.2K Pull-up
GPIO10	OUT	N/A	
GPIO11	OUT	-	GPU Core VDD PWM control signal
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	Phase Shedding
GPIO14	IN	N/A	
GPIO15	IN	N/A	
GPIO16		N/A	
GPIO17	IN	N/A	
GPIO18	IN	N/A	
GPIO19	IN	N/A	
GPIO20		N/A	
GPIO21	OUT		GPU PCIe self-reset control
OVERT	OUT		Active Low Thermal Catastrophic Over Temperature

Performance Mode P0 TDP at Tj = 102 C\* (DDR3)

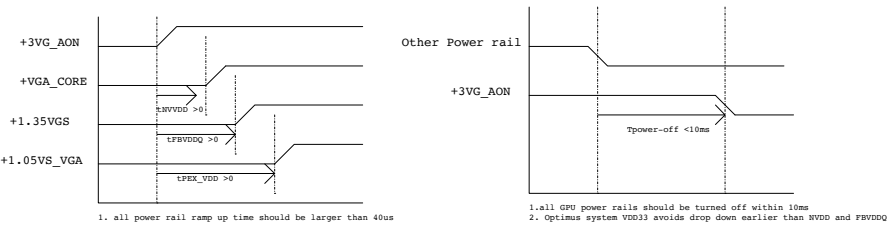
Products	GPU (4)	Mem (1.5)	NVCLK /MCLK	NVVDD			FBVDD (1.35V)		FBVDDQ (GPU+Mem) (1.35V)		PCI Express (1.05V)		I/O and PLLVDD (1.05V)		Other (3.3V)	
	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N14X 128bit 2GB DDR3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

N15x Multi-level Straps

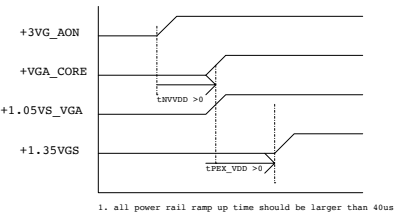
Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

N15V-GM Power Sequence



N15S-GT Power Sequence

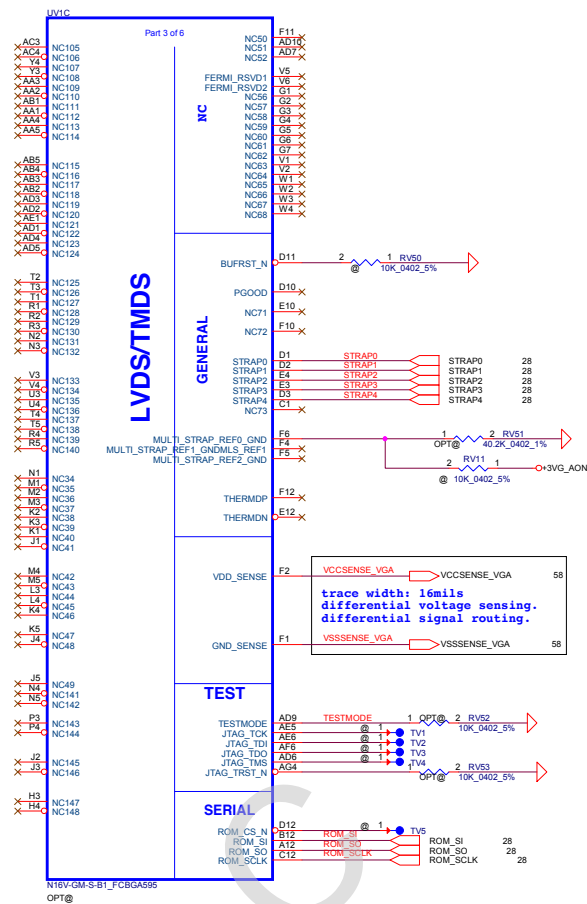


N15x Binary Straps

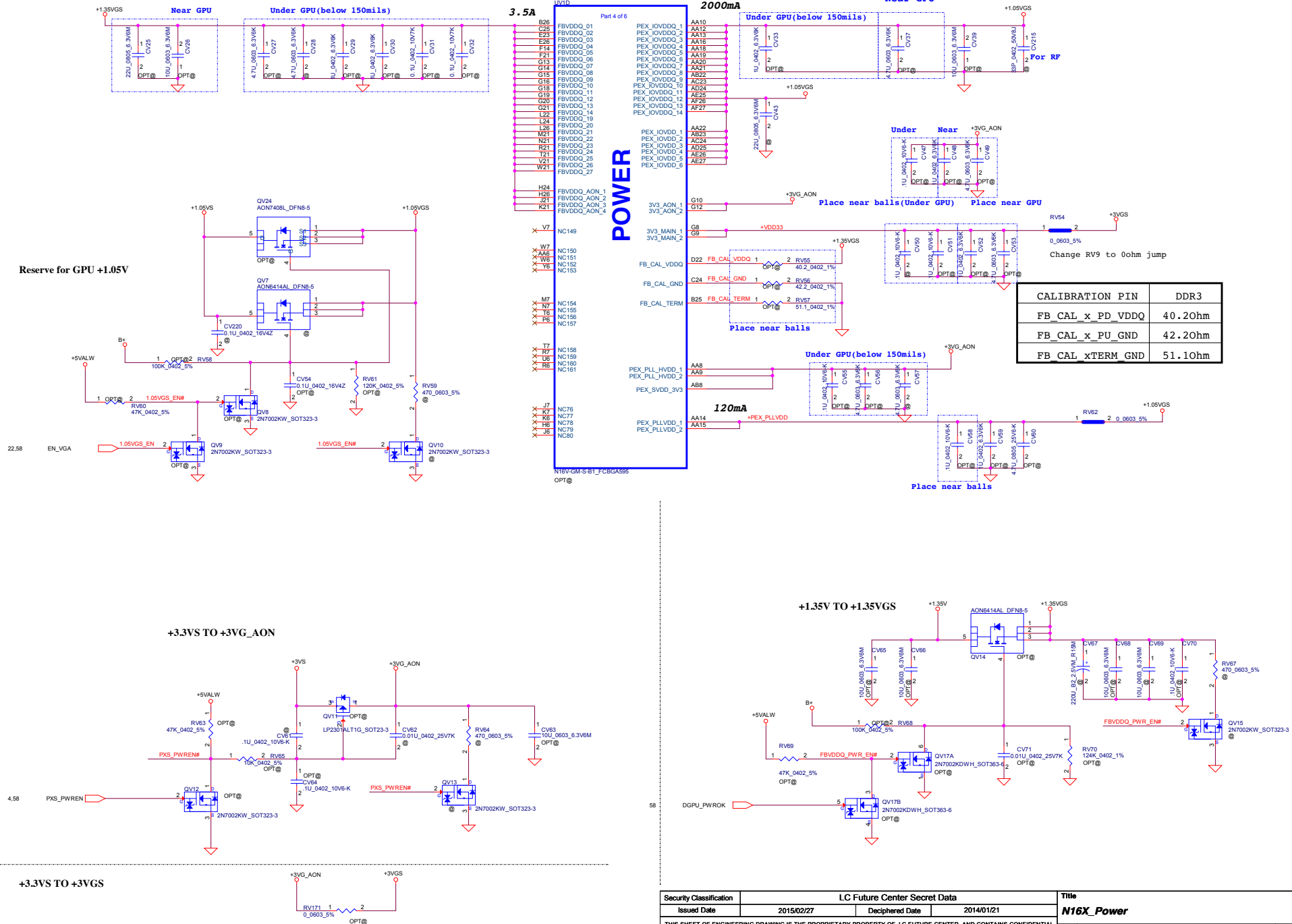
Physical Strapping pin	Power Rail	Strap Mapping
ROM_SCLK	+3VGS	SMB_ALT_ADDR
ROM_SI	+3VGS	SUB_VENDOR
ROM_SO	+3VGS	VGA_DEVICE
STRAP0	+3VGS	RAM_CFG[0]
STRAP1	+3VGS	RAM_CFG[1]
STRAP2	+3VGS	RAM_CFG[2]
STRAP3	+3VGS	RAM_CFG[3]
STRAP4	+3VGS	PCIE_MAX_SPEED

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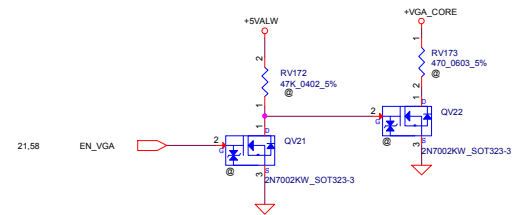
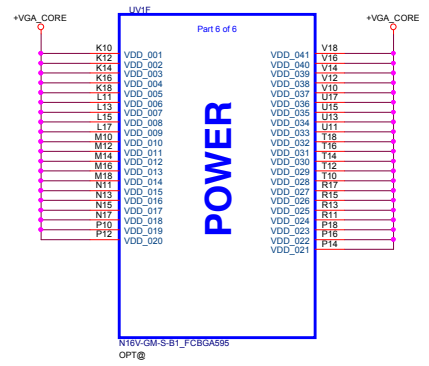
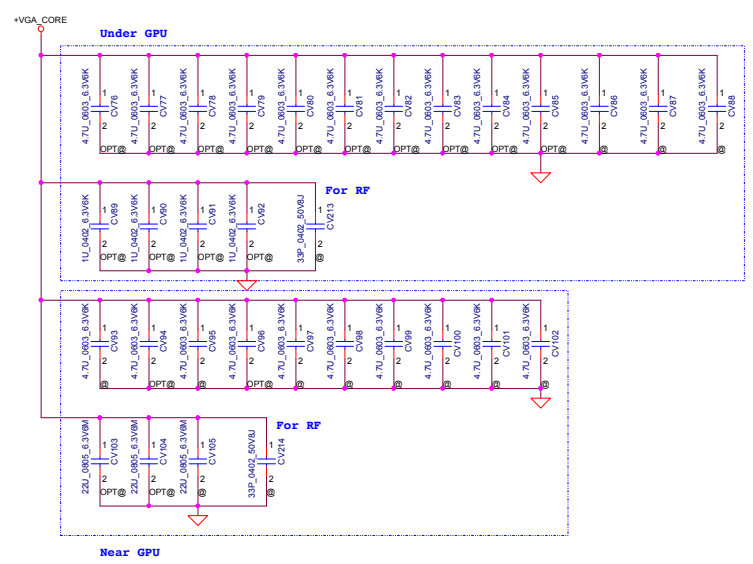
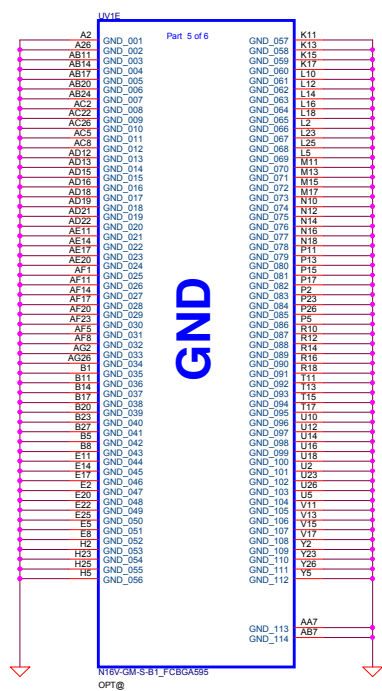




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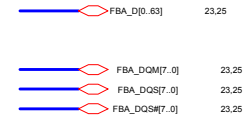
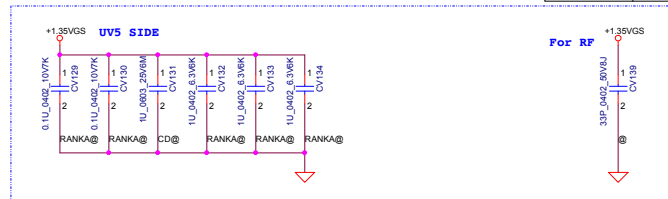
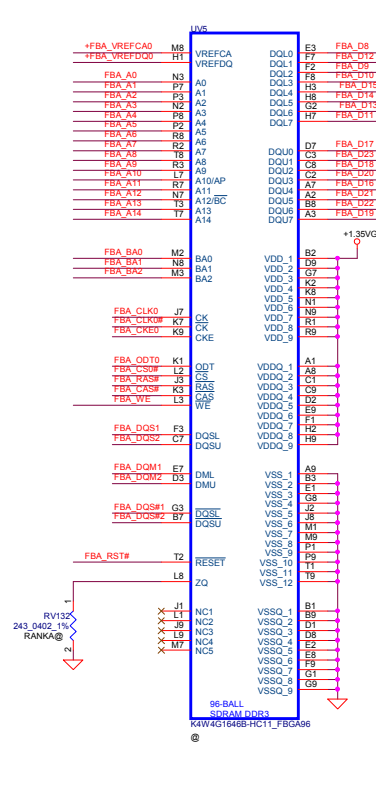
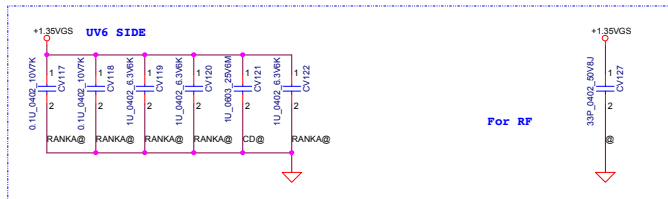
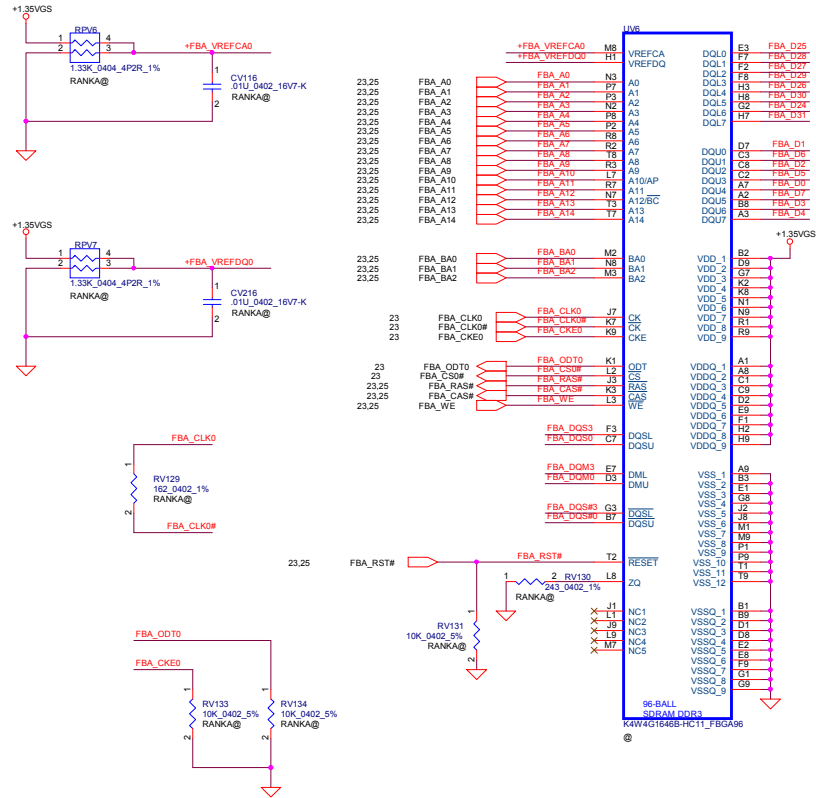
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at least 16 mils width(optimal)  
20 mils spacing to other signals /planes



### CMD mapping mod Mode D

Address	Rank0	Rank1
FBX_CMD0	CS0#	
FBX_CMD1		
FBX_CMD2	ODT0	
FBX_CMD3	CKE0	
FBX_CMD4	A14	A14
FBX_CMD5	RST	RST
FBX_CMD6	A9	A9
FBX_CMD7	A7	A7
FBX_CMD8	A2	A2
FBX_CMD9	A0	A0
FBX_CMD10	A4	A4
FBX_CMD11	A1	A1
FBX_CMD12	BA0	BA0
FBX_CMD13	WE	WE
FBX_CMD14	A15	A15
FBX_CMD15	CAS#	CAS#
FBX_CMD16	CS1#	
FBX_CMD17		
FBX_CMD18	ODT1	
FBX_CMD19	CKE1	
FBX_CMD20	A13	A13
FBX_CMD21	A8	A8
FBX_CMD22	A6	A6
FBX_CMD23	A11	A11
FBX_CMD24	A5	A5
FBX_CMD25	A3	A3
FBX_CMD26	BA2	BA2
FBX_CMD27	BA1	BA1
FBX_CMD28	A12	A12
FBX_CMD29	A10	A10
FBX_CMD30	RAS#	RAS#
FBX_CMD31		
FBX_CMD32		
FBX_CMD33		
FBX_CMD34	DBG0	
FBX_CMD35	DBG1	



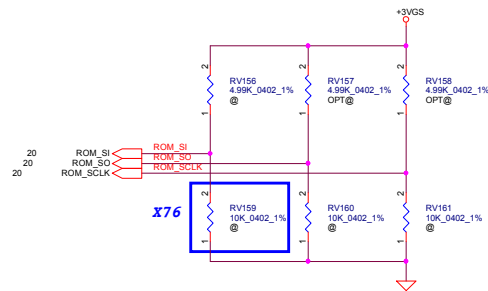
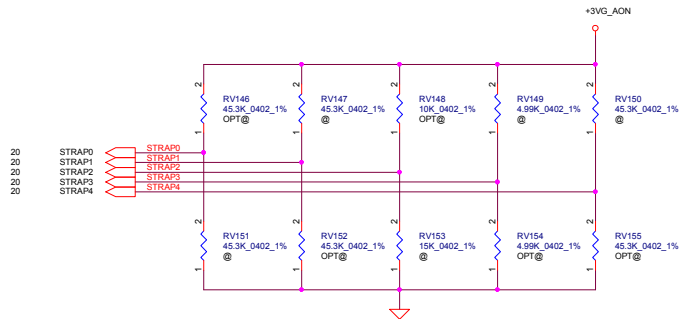


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						Size	Document Number	Rev
						Custom	CG510	0.2
						Date: Saturday, May 09, 2015		



Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

Resistor Values	Pull-up to +3VGS	Pull-down to Gnd
4.99K	1000	0000
SD0344918J	1001	0001
10K	1010	0010
15K	1011	0011
20K	1100	0100
24.9K	1101	0101
SD0344528J	1110	0110
30.1K	1111	0111
SD0340128J		
34.8K		
SD0344828J		
45.3K		
SD03445328J		

Physical Strapping pin	Power Rail	Strap Mapping
ROM_SCLK	+3VGS	SMB_ALT_ADDR
ROM_SI	+3VGS	SUB_VENDOR
ROM_SO	+3VGS	VGA_DEVICE
STRAP0	+3VGS	RAM_CFG[0]
STRAP1	+3VGS	RAM_CFG[1]
STRAP2	+3VGS	RAM_CFG[2]
STRAP3	+3VGS	RAM_CFG[3]
STRAP4	+3VGS	PCIE_MAX_SPEED

DEVID_SEL	
0	(Default)
1	

PCIE_CFG	
0	(Default)
1	

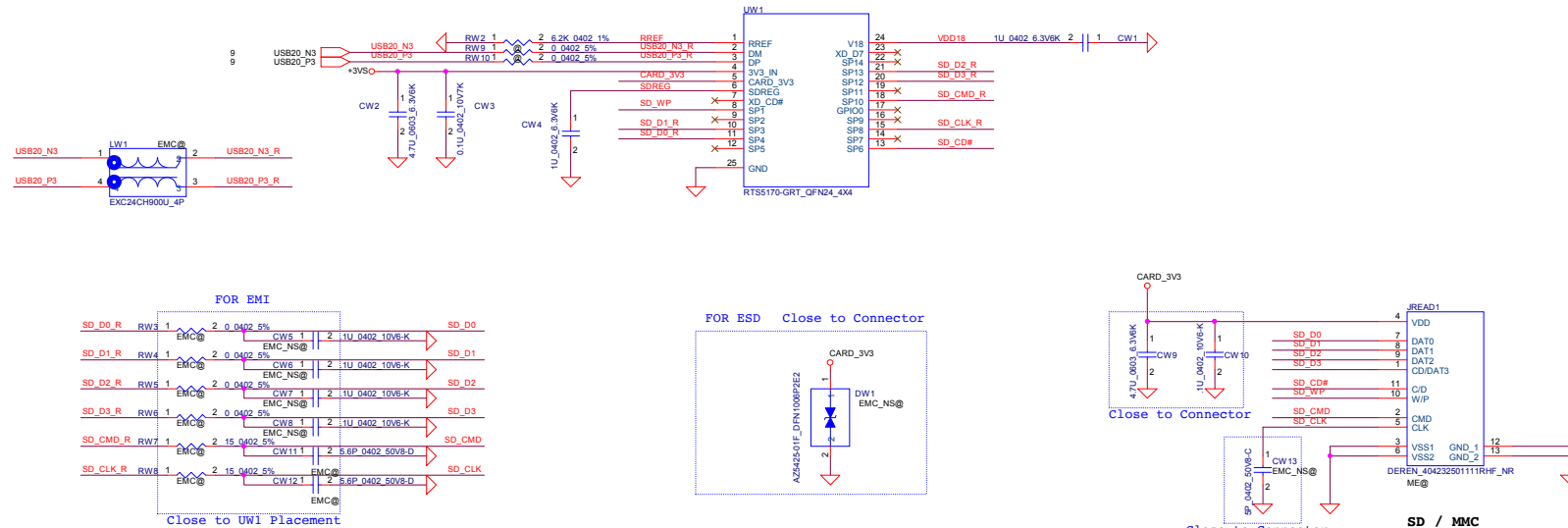
SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

X76									
GPU	FB Memory (DDR3L)	ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N16V-GM	H5TC4G63AFR-11C	0xE	PU 4.99K	PU 4.99K	PU 45.3K	PD 45.3K	PU 10K	PD 4.99K	PD 45.3K
	Hynix 900MHz 256M x 16	PU 34.8K							
	MT41J256M16HA-093G:E	0xD							
	Micron 900MHz 256M x 16	PU 30.1K							
	H5TC2G63FPR-11C	0xB							
	Hynix 900MHz 128M x 16	PU 20K							
	MT41J128M16JT-093G	0x8							
	Micron 900MHz 128M x 16	PU 4.99K							
Samsung 900MHz	K4W2G1646Q-BC1A	0x7	PD 45.3K						
	128M x 16								

VRAM	X76	VRAM P/N
Samsung	X7606012101	SA00005SH40
Micron	X7606012001	SA00005M120
Hynix	X7606012002	SA00005VS00

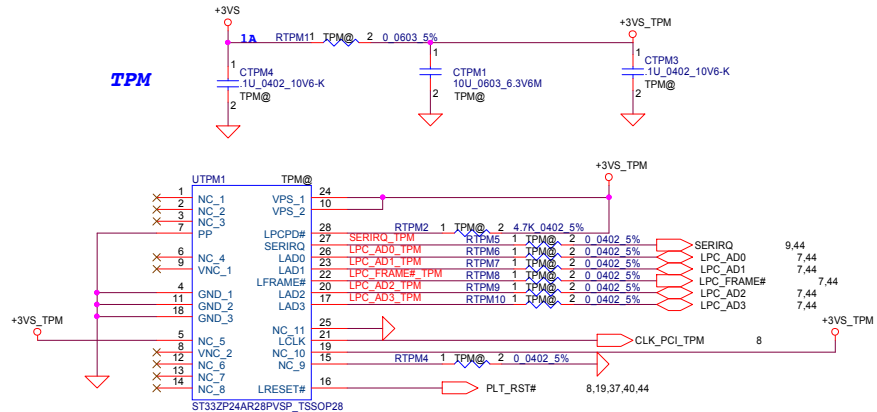
5					4					3					2					1				
D																								
C																								
B																								
A																								
5					4					3					2					1				



CW11,CW12 need to change 5.6pf CAP as EMC request

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Sheet	Document Number	Rev	
1	CG510	0.2	
Date	Saturday, May 08, 2016	Sheet	30 of 60

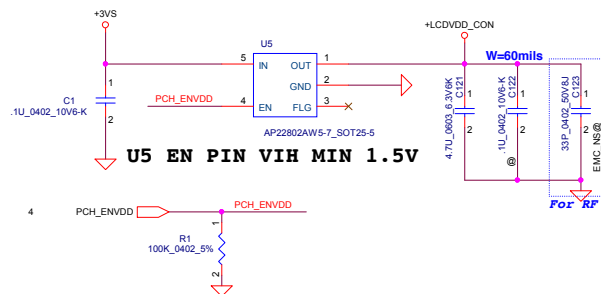
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				Custm	CG510	0.2
Date: Saturday, May 09, 2015				Sheet	31	of 59



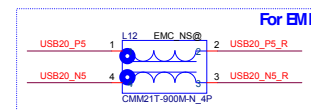
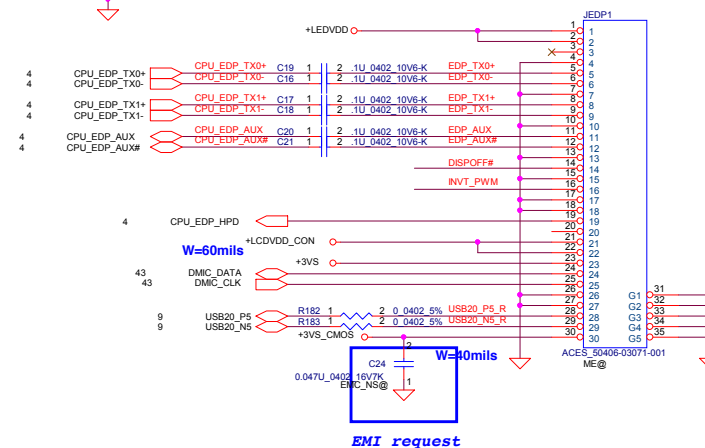
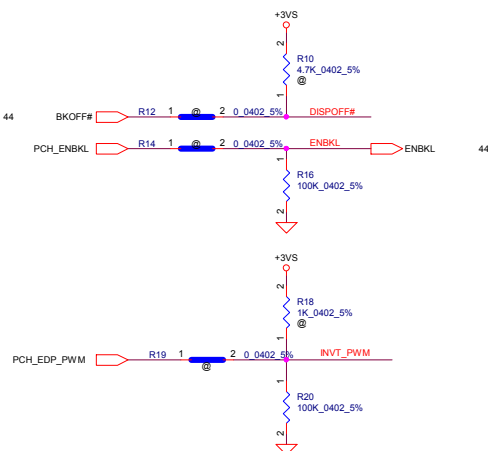
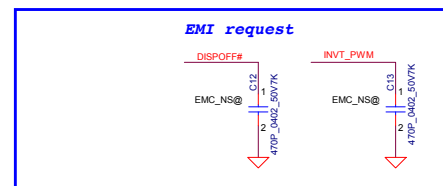
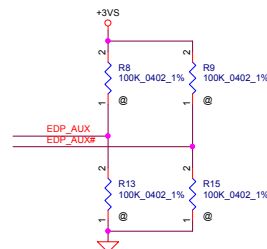
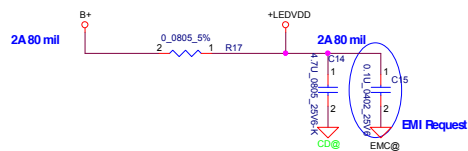
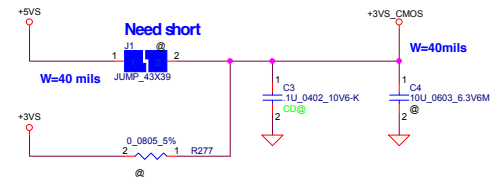
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Issued Date		2015/02/27	Deciphered Date	2013/08/05	TPM
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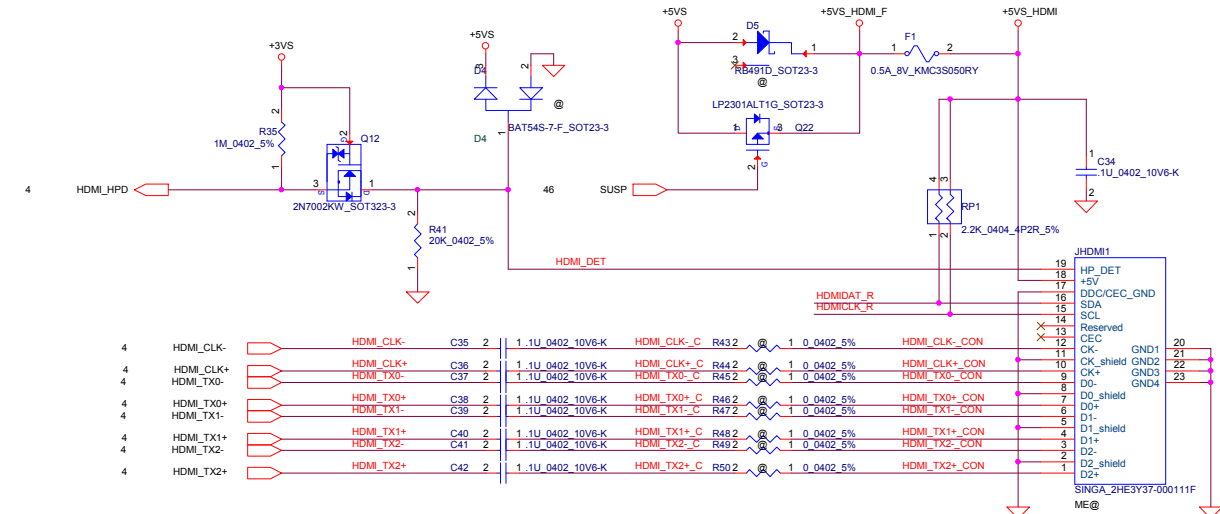
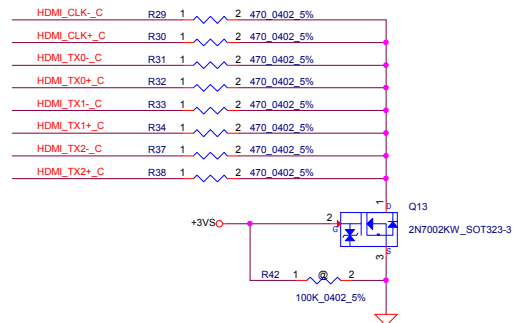
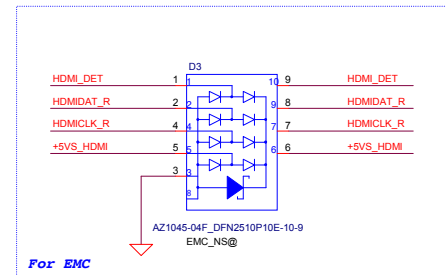
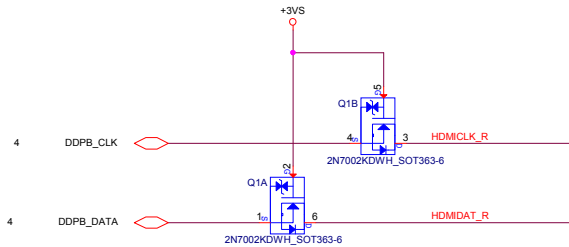
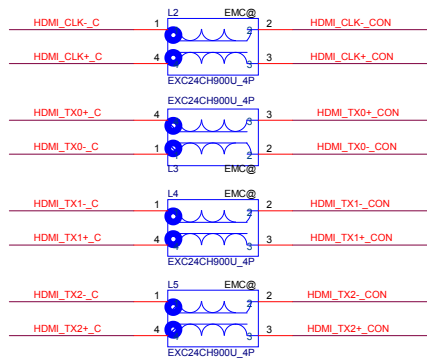
## LCD POWER CIRCUIT



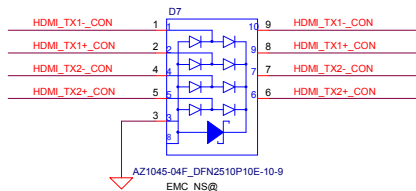
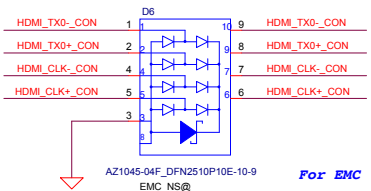
## CMOS Camera



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Close to JHDMI1



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						Date:		Saturday, May 09, 2015		Sheet	

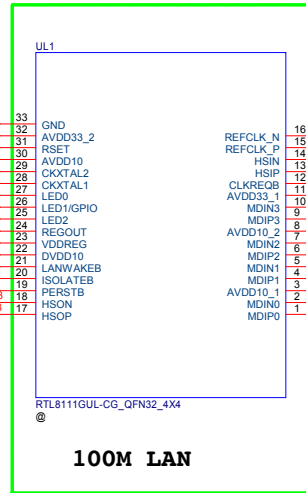
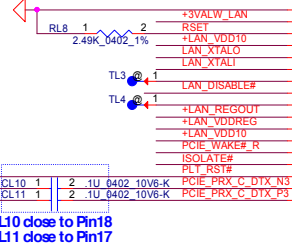
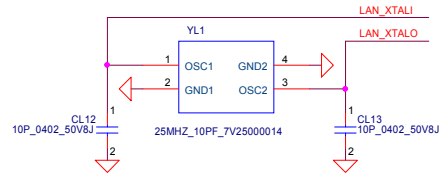
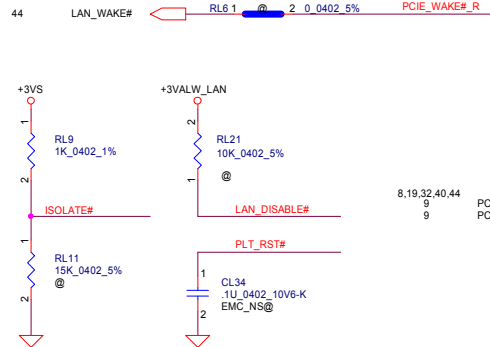
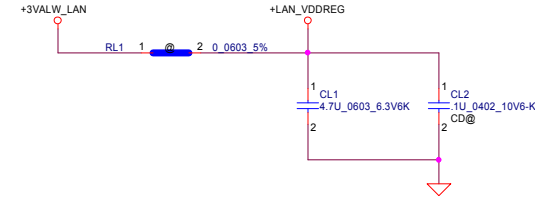
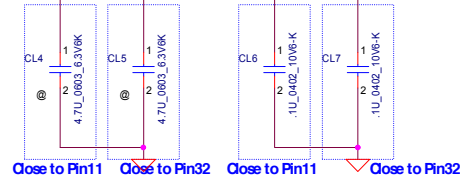
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+3VALW TO +3VALW\_LAN

Need short

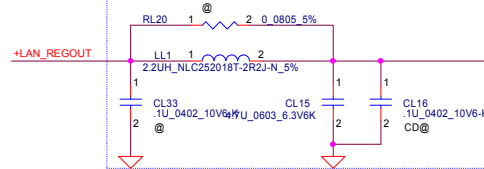
+3VALW\_LAN rising time (10%~90%):  
0.5ms < spec < 100ms

width : 40 mils

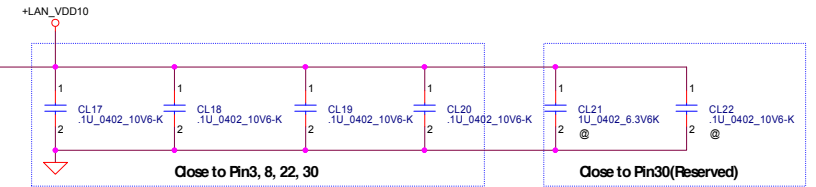


100M LAN

For RTL8111GUL/ RTL8106EUL(SWRmode)

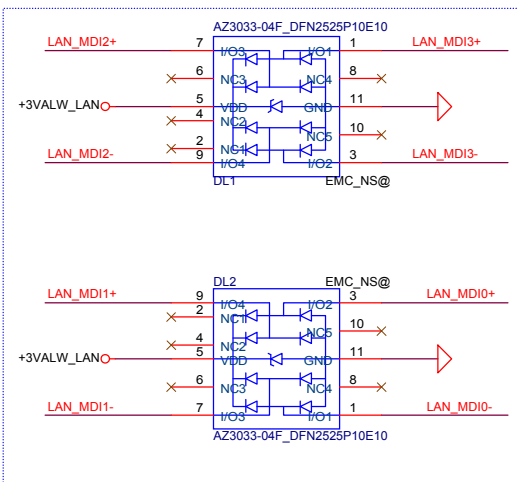


Layout Note: LL1 must be within 200mil to Pin24,  
CL15, CL16 must be within 200mil to LL1  
+LAN\_REGOUT: Width =60mil

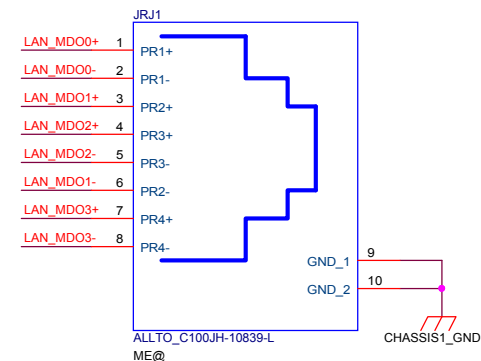
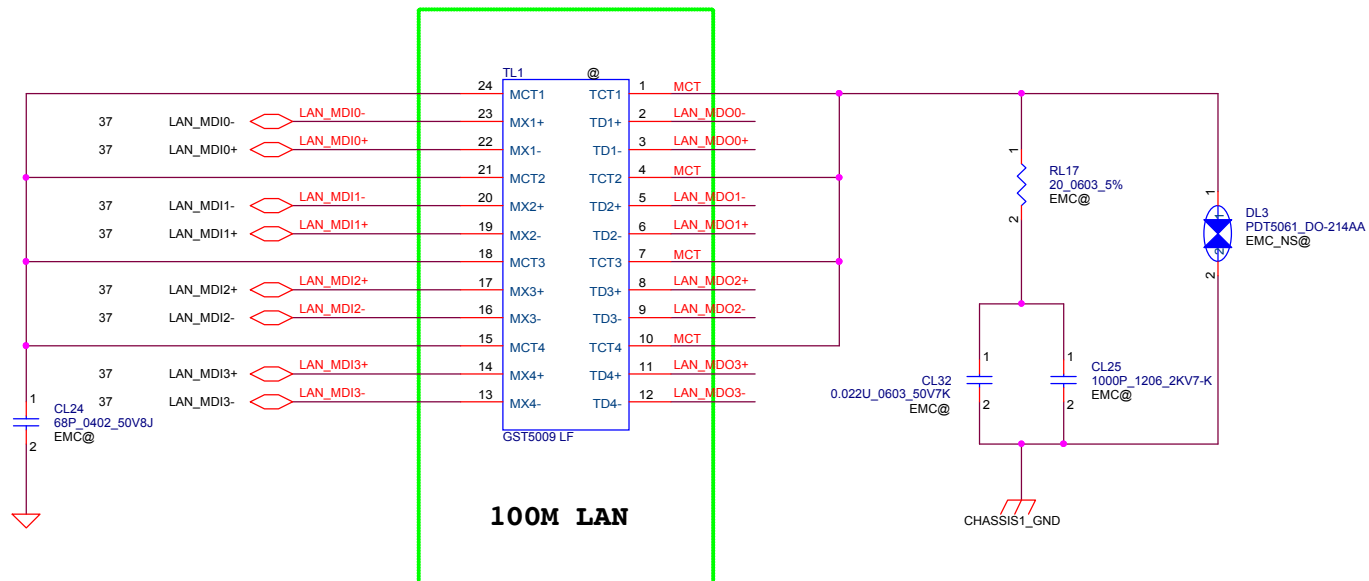
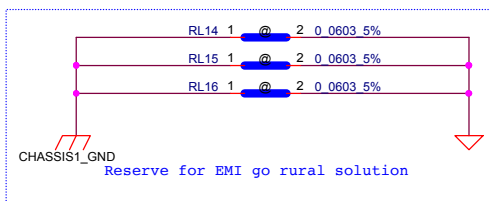


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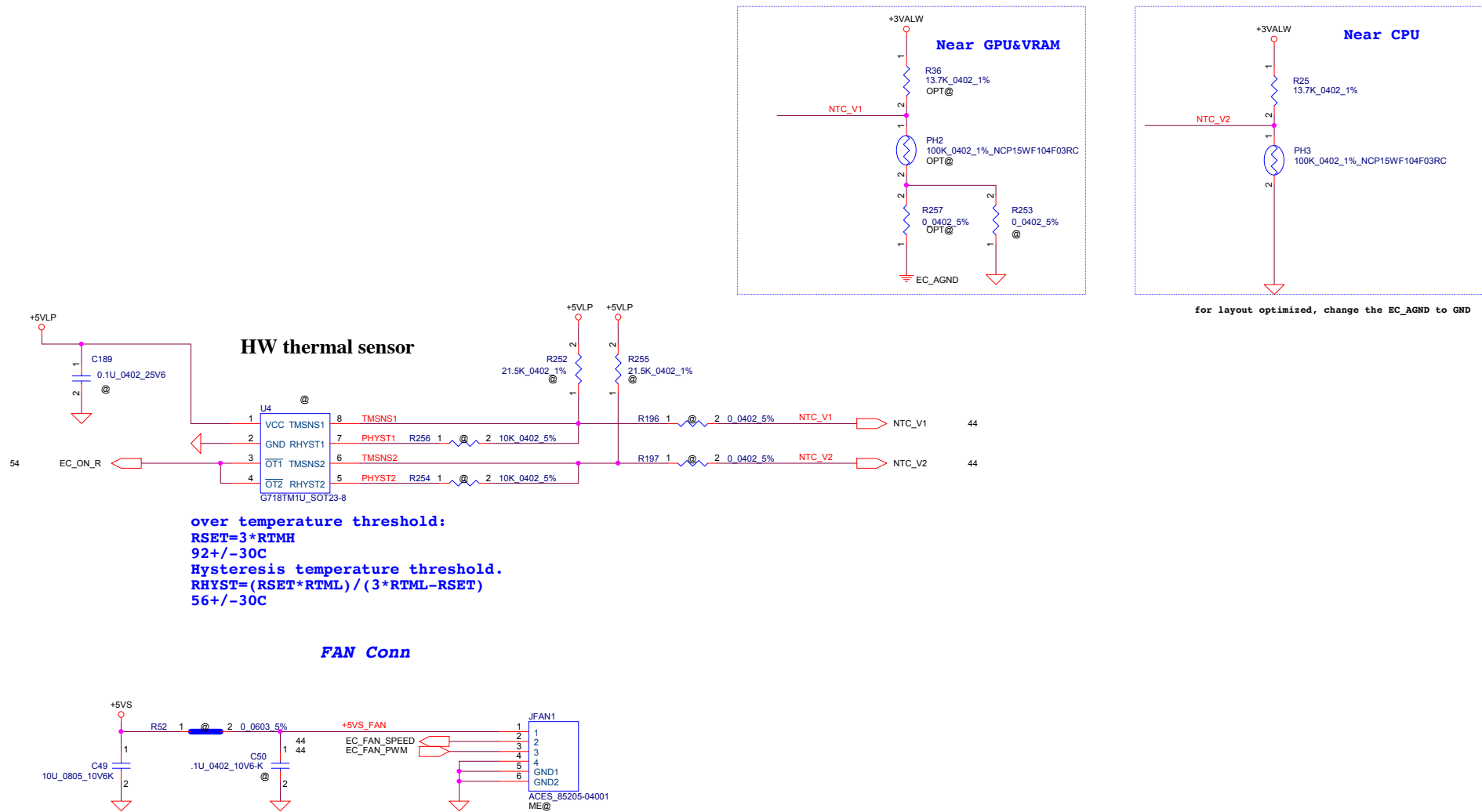
DL1/DL2  
1'S PN:SC300003M00



Place Close to TL1

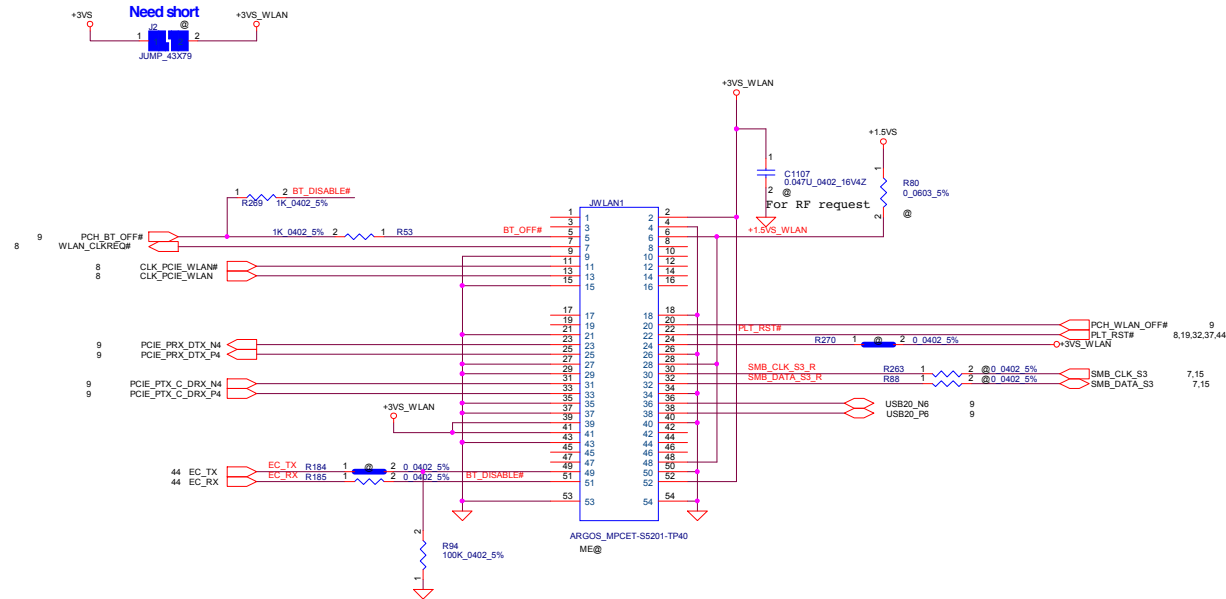


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				Date: Saturday, May 09, 2015	Sheet 39 of 59

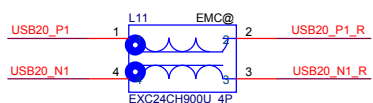
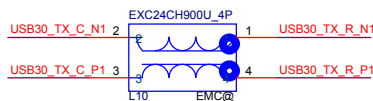
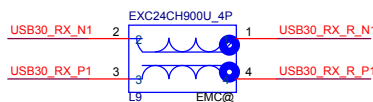
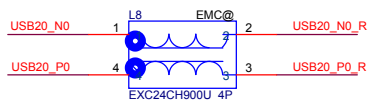
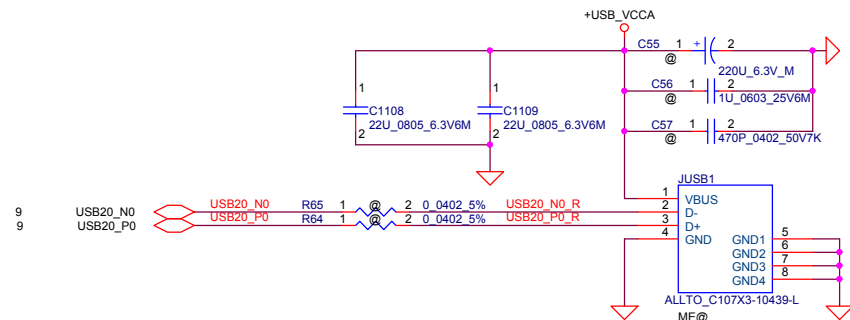
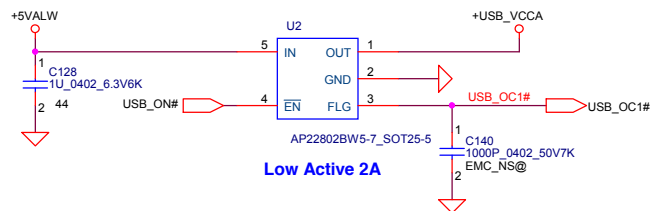
# Mini-Express Card(WLAN/WiMAX)



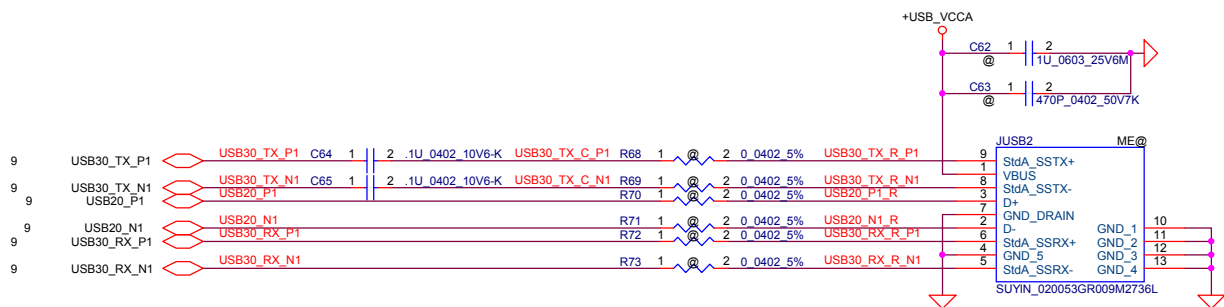
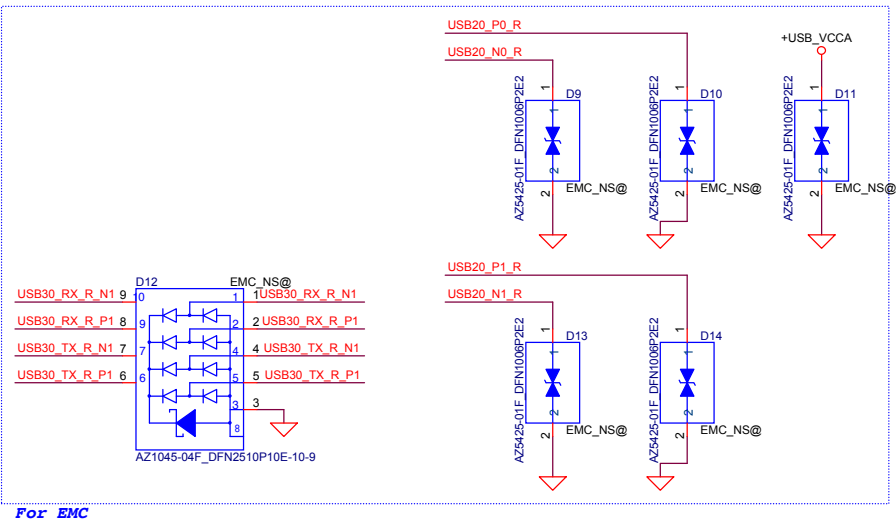
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## LEFT SIDE USB PORT X2

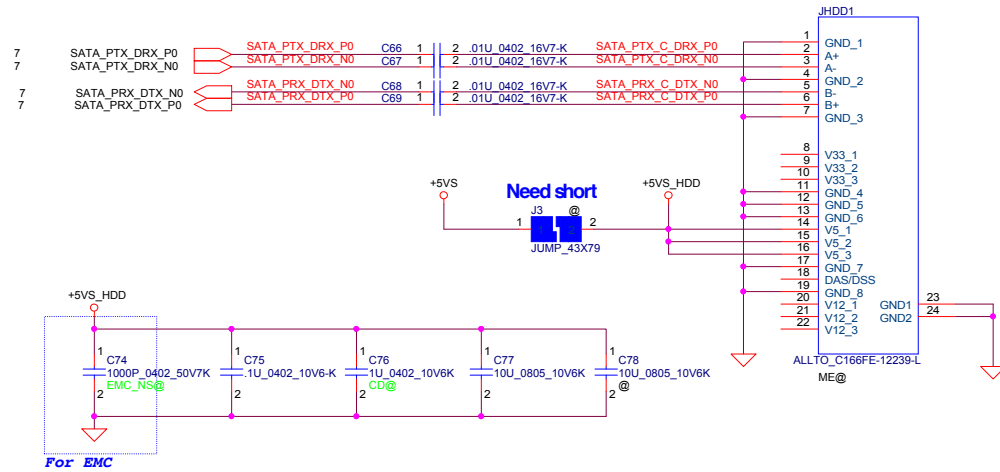


*For EMC*

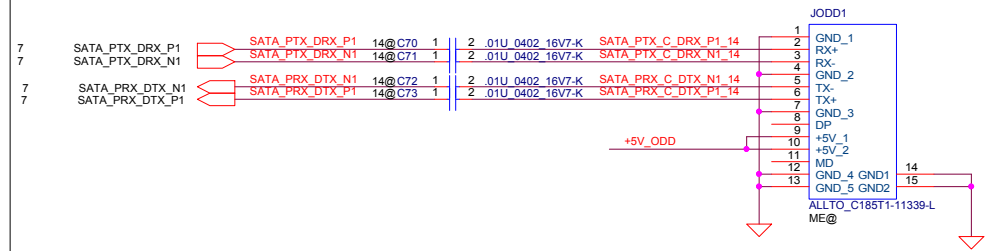


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Issued Date	2015/02/27	Deciphered Date	2013/08/05	<b>USB2.0/USB3.0 PORT (LEFT)</b> Size Custom <b>CG510</b> Rev 0.2	
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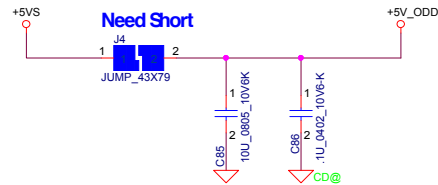
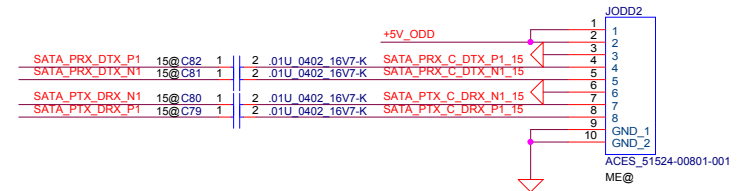
# SATA HDD Conn.



# FOR 14" SATA ODD Conn.

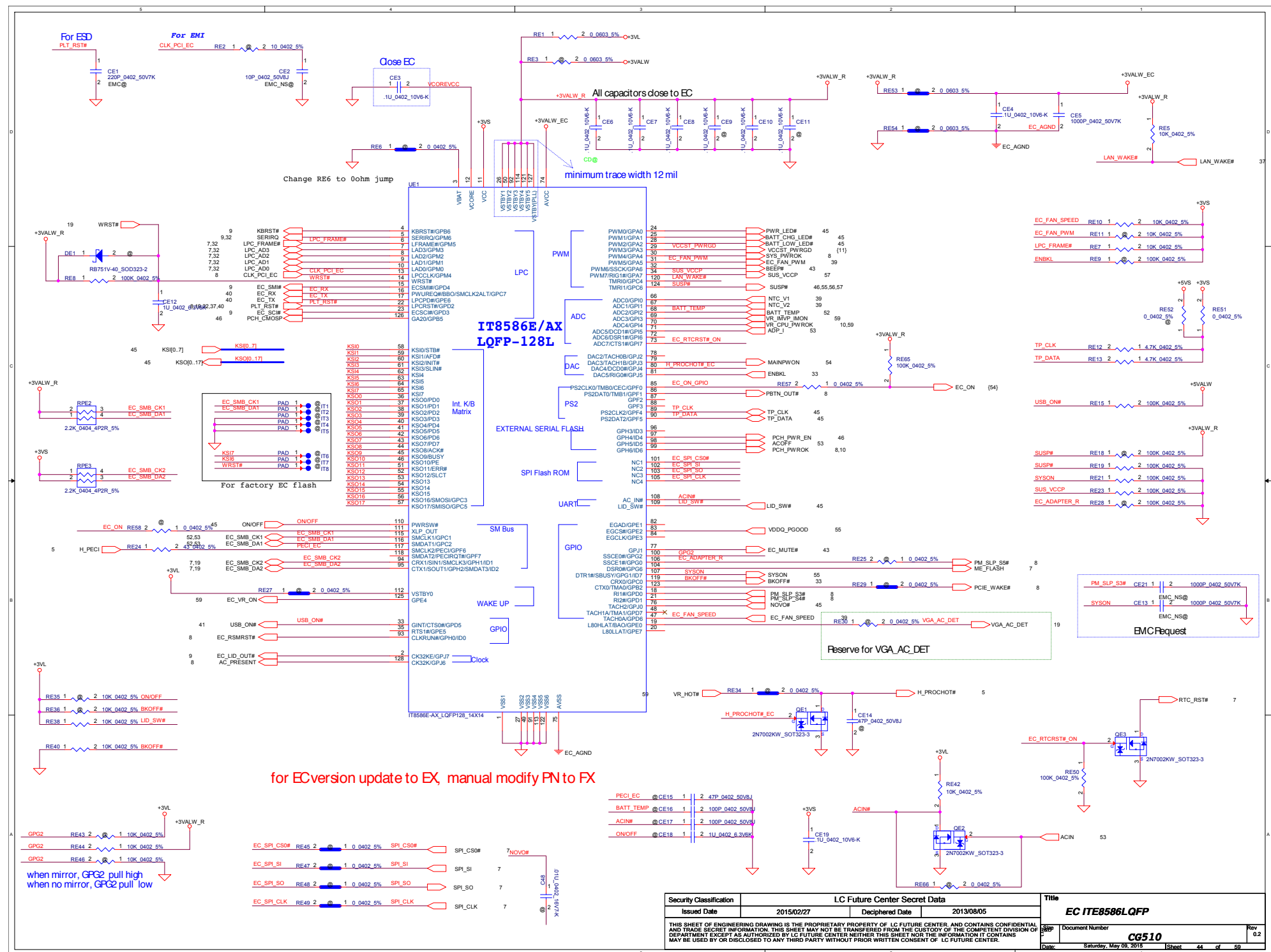


# FOR 15" SATA ODD FFC Conn

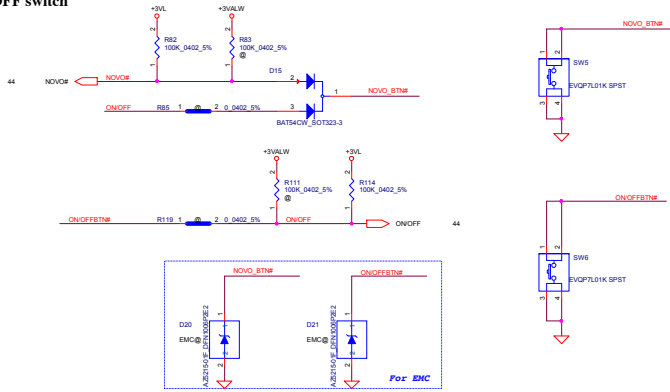


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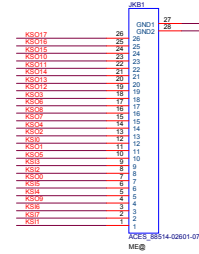
# ON/OFF switch



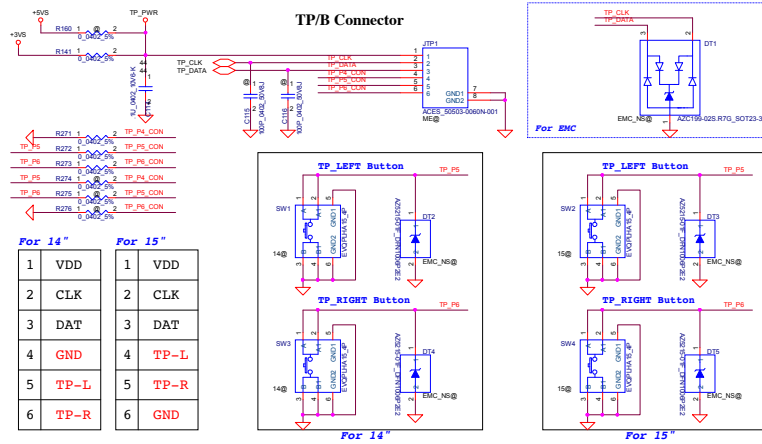
# K/B Connector



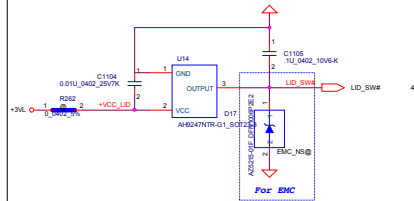
15"



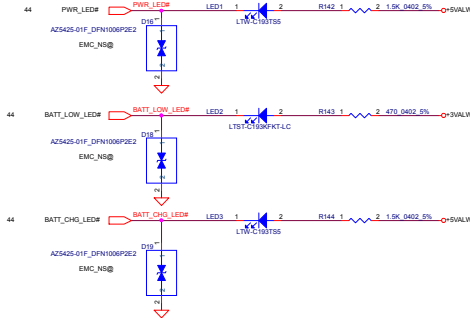
# TP/B Connector



# Hall Sensor



# LED



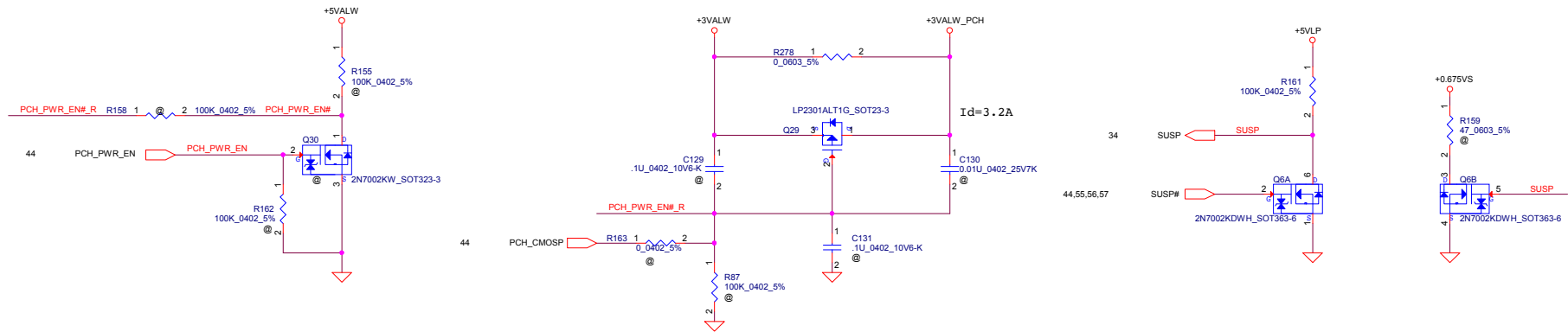
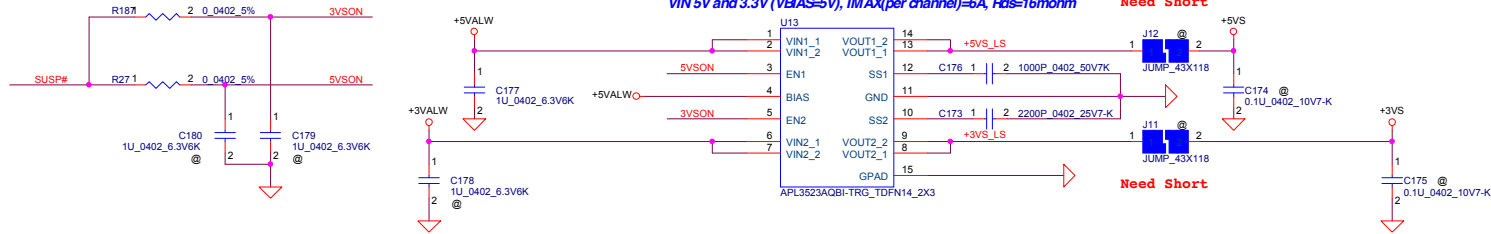
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Issued Date	2015/02/27	Deciphered Date	2013/08/05	KBD/PWR/LED/TP Conn.	
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				Date	Wednesday, May 13, 2015
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# **Load Switch** **+5VALW To +5VS** **+3VALW To +3VS**

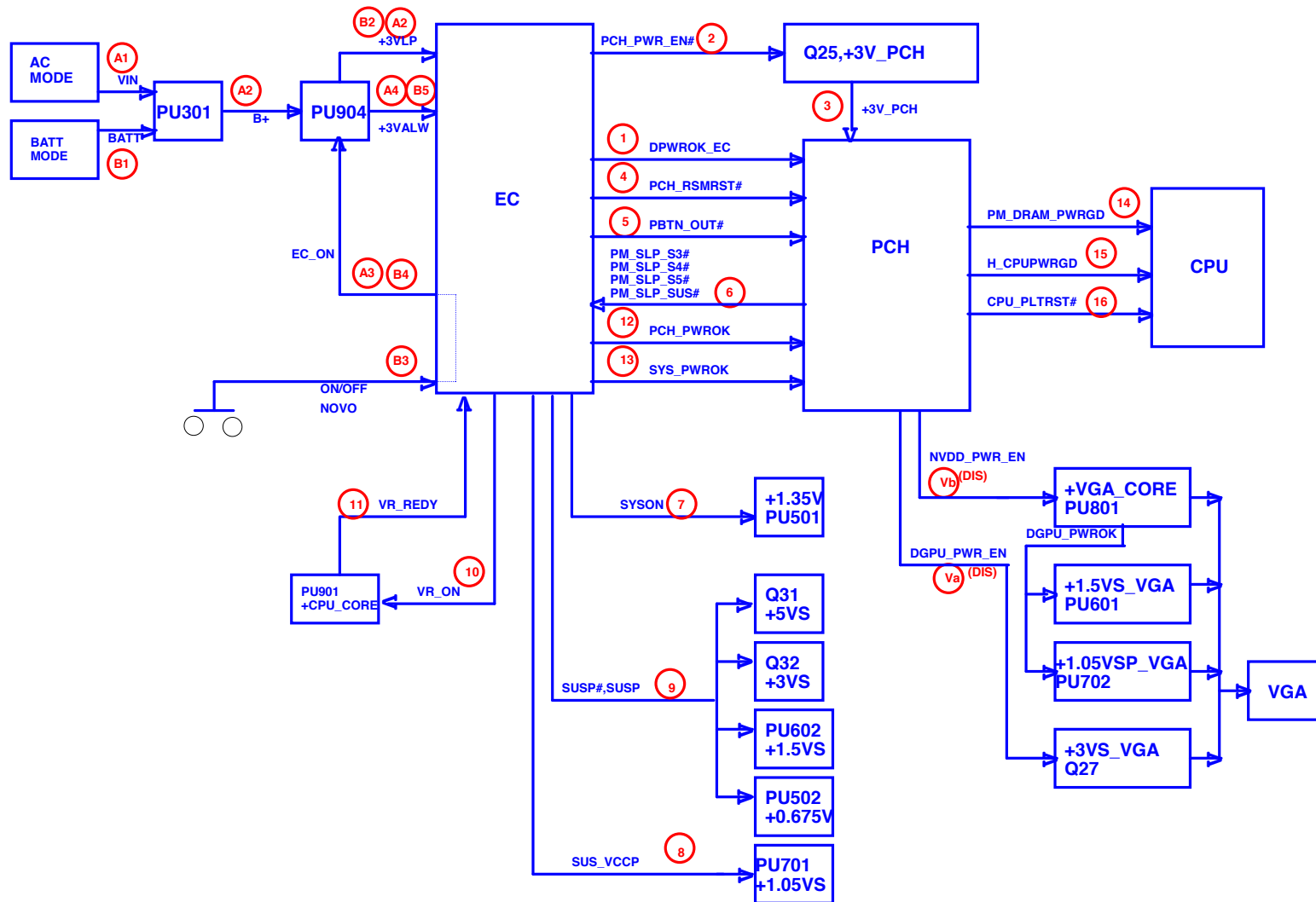
**+3VS C173 --> 2.74ms**  
**+5VS C176 --> 2.03ms**

VIN 5V and 3.3V (VBias=5V), I<sub>MAX</sub>(per channel)=6A, R<sub>ds</sub>=16mohm

**Need Short**



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								Date:	Thursday, May 14, 2015		ISheet
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				Rev 0.2
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5

4

3

2

1

D

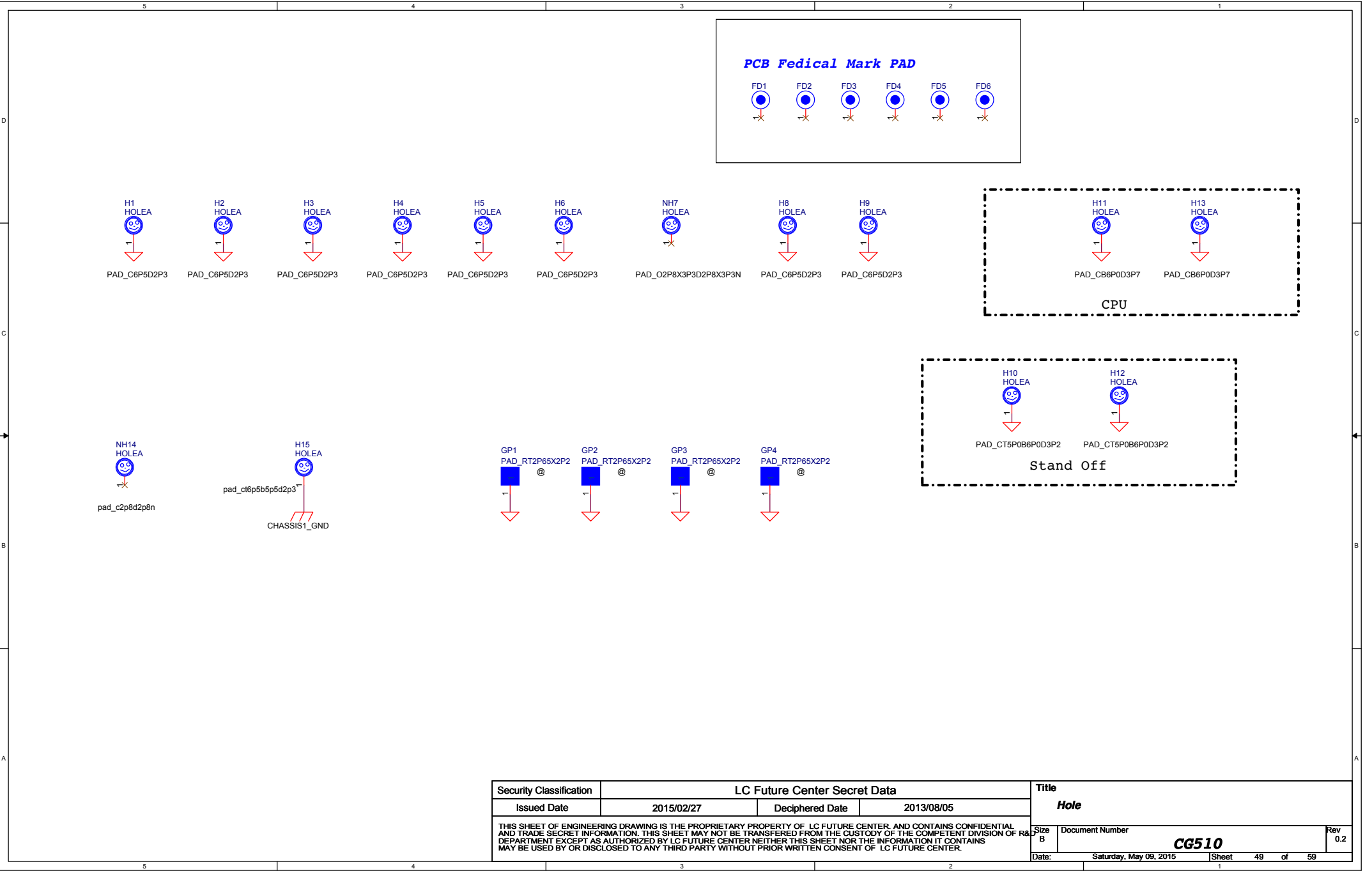
C

B

A

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			0.1
			Friday, May 15, 2015
			Sheet 48 of 59

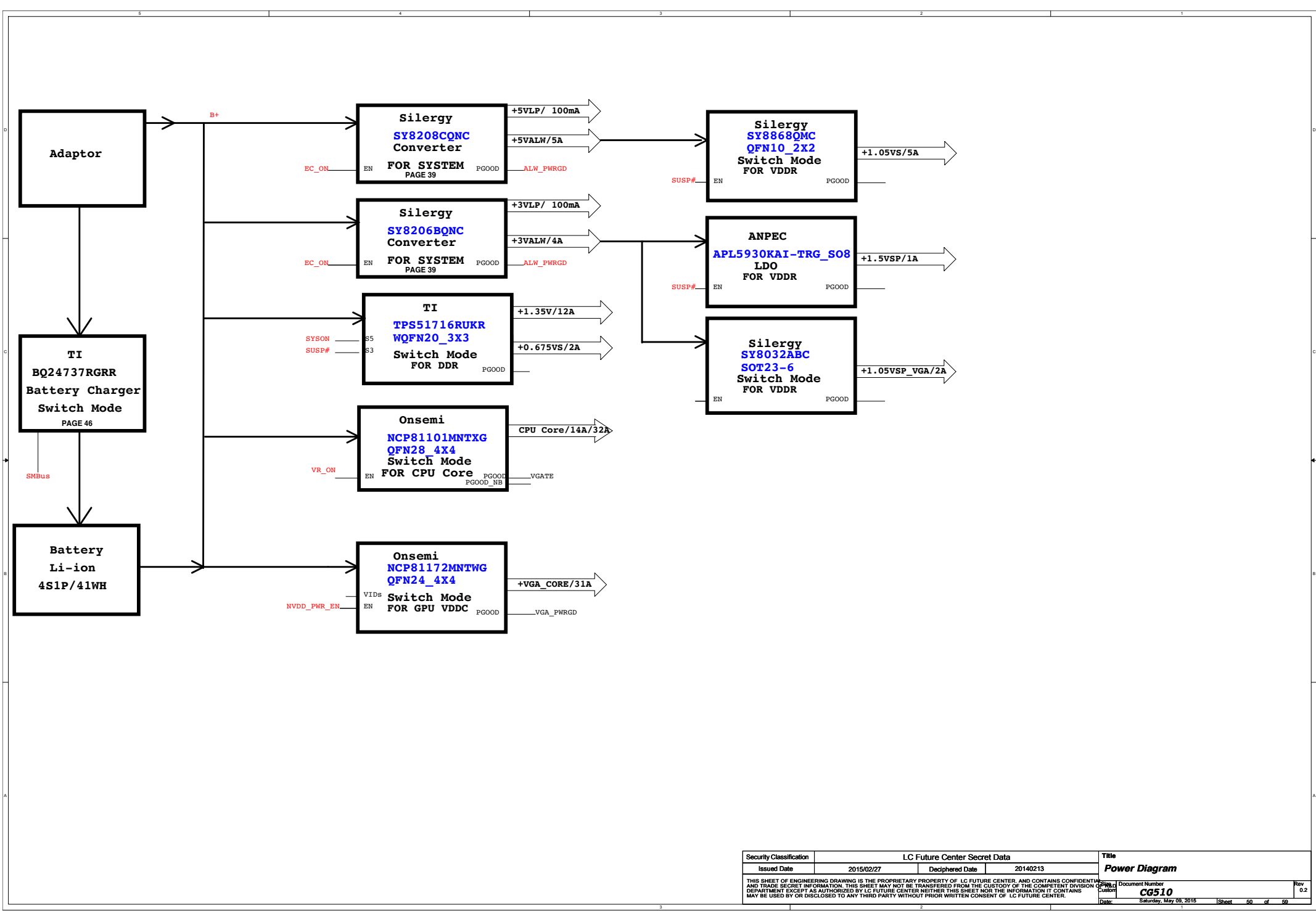


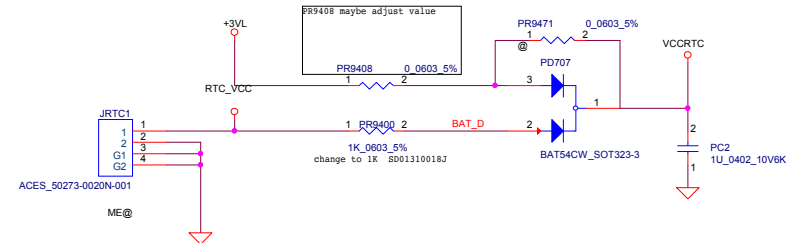
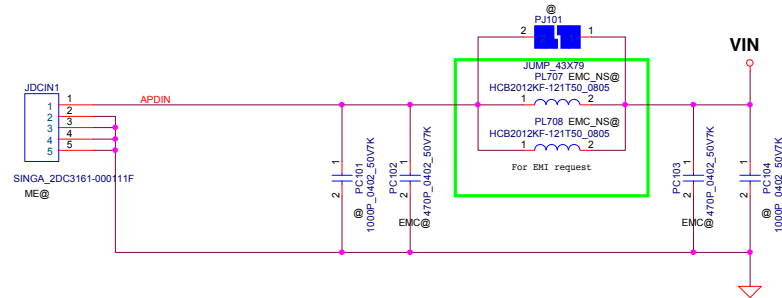


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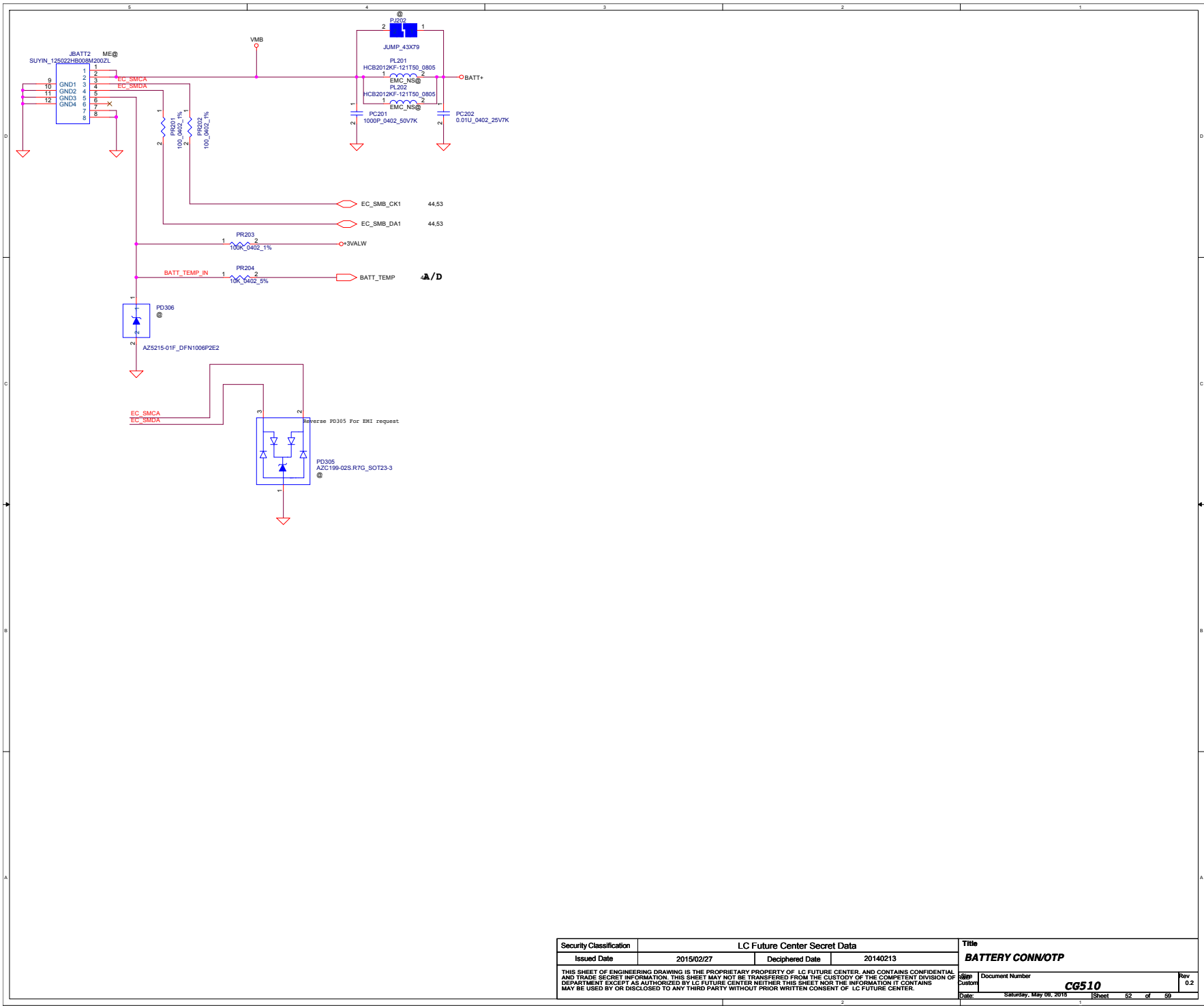
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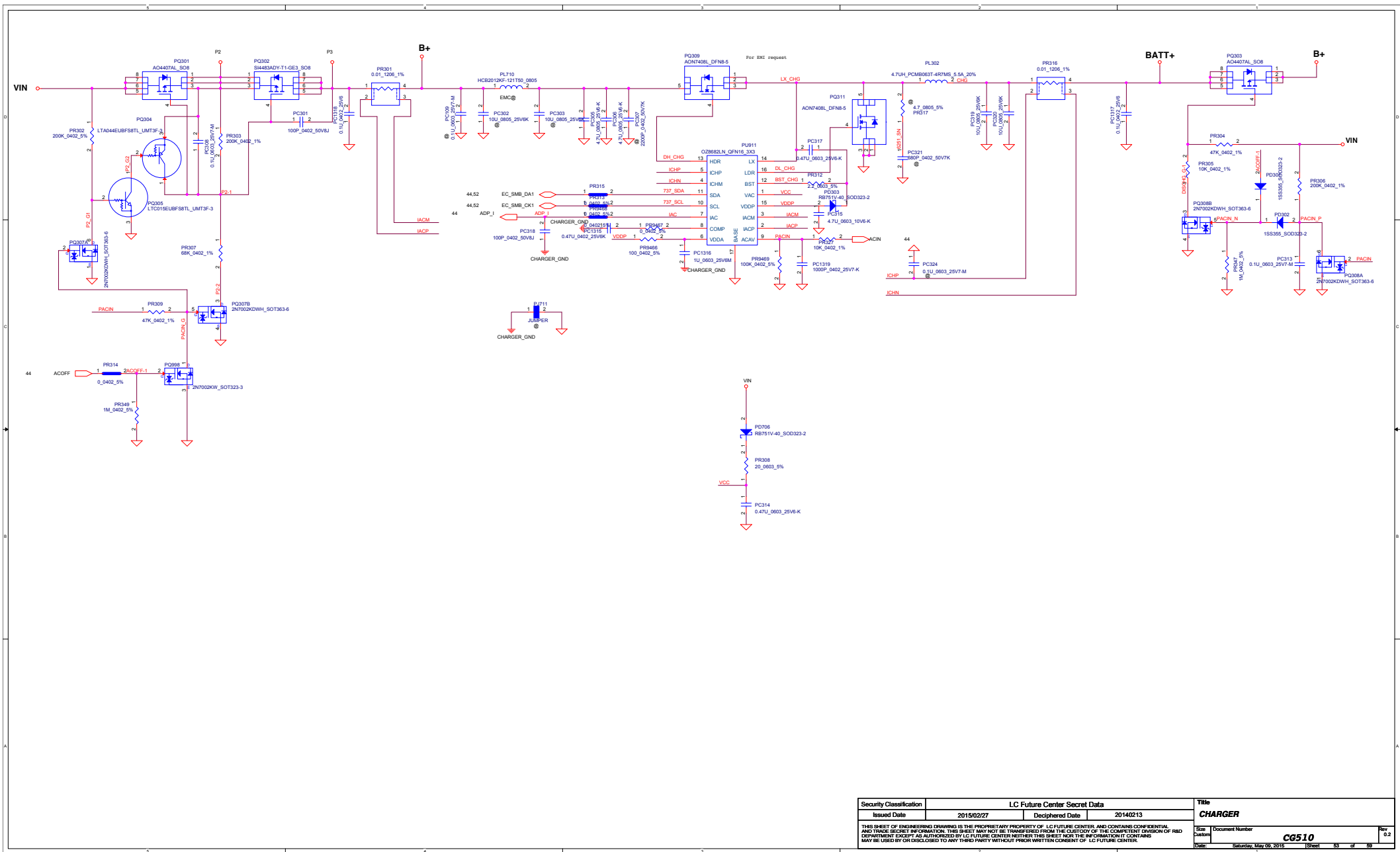
Rev 0.2



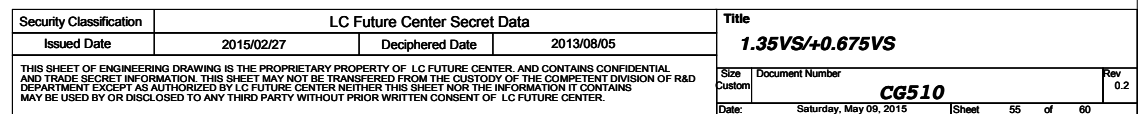


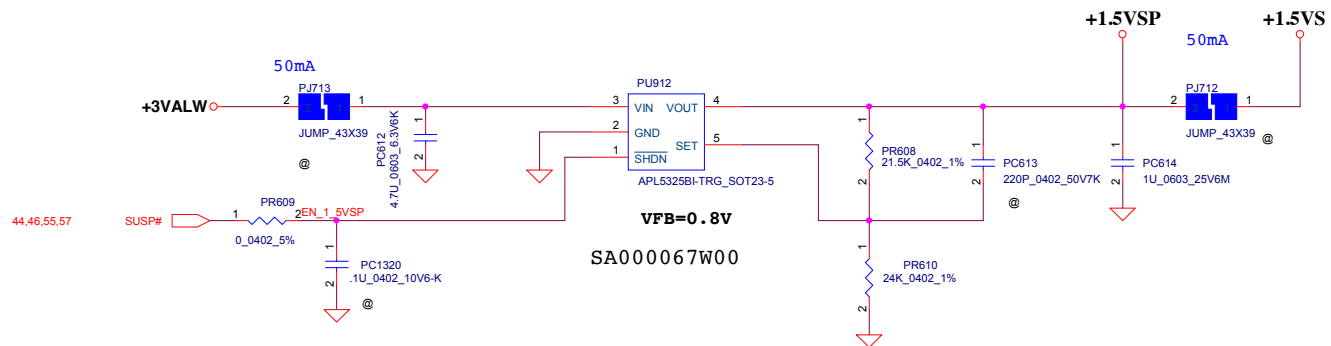
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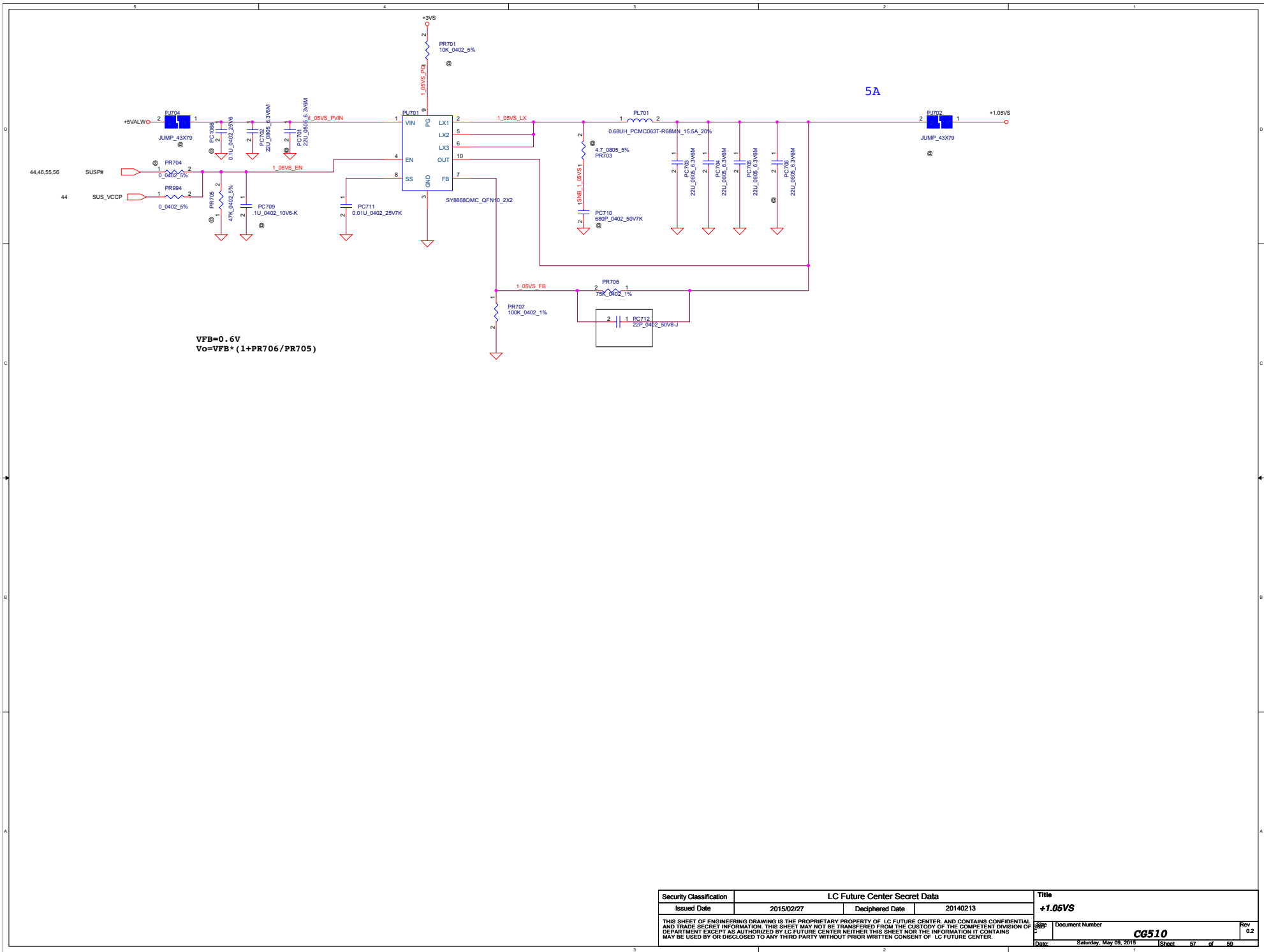




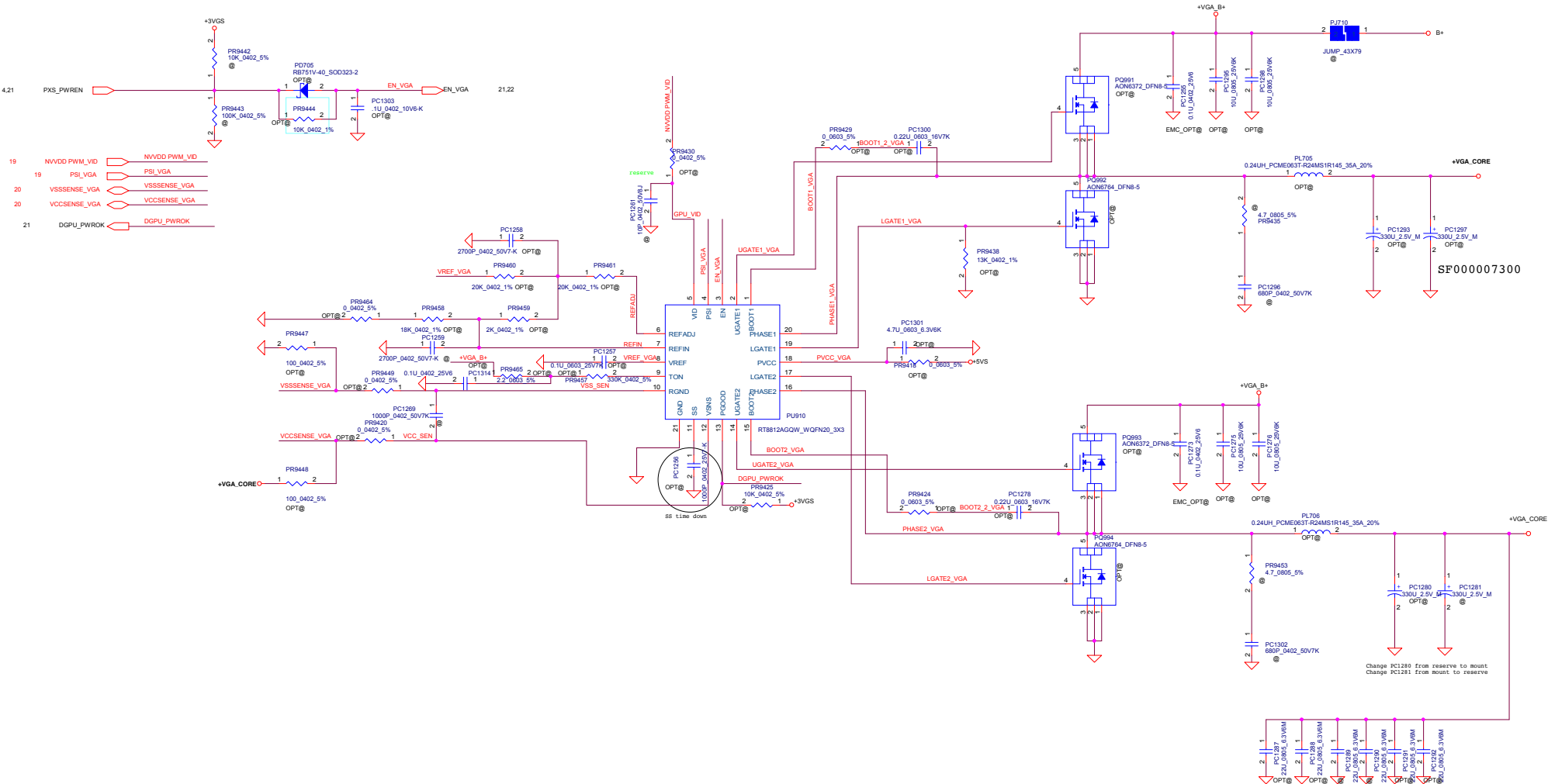


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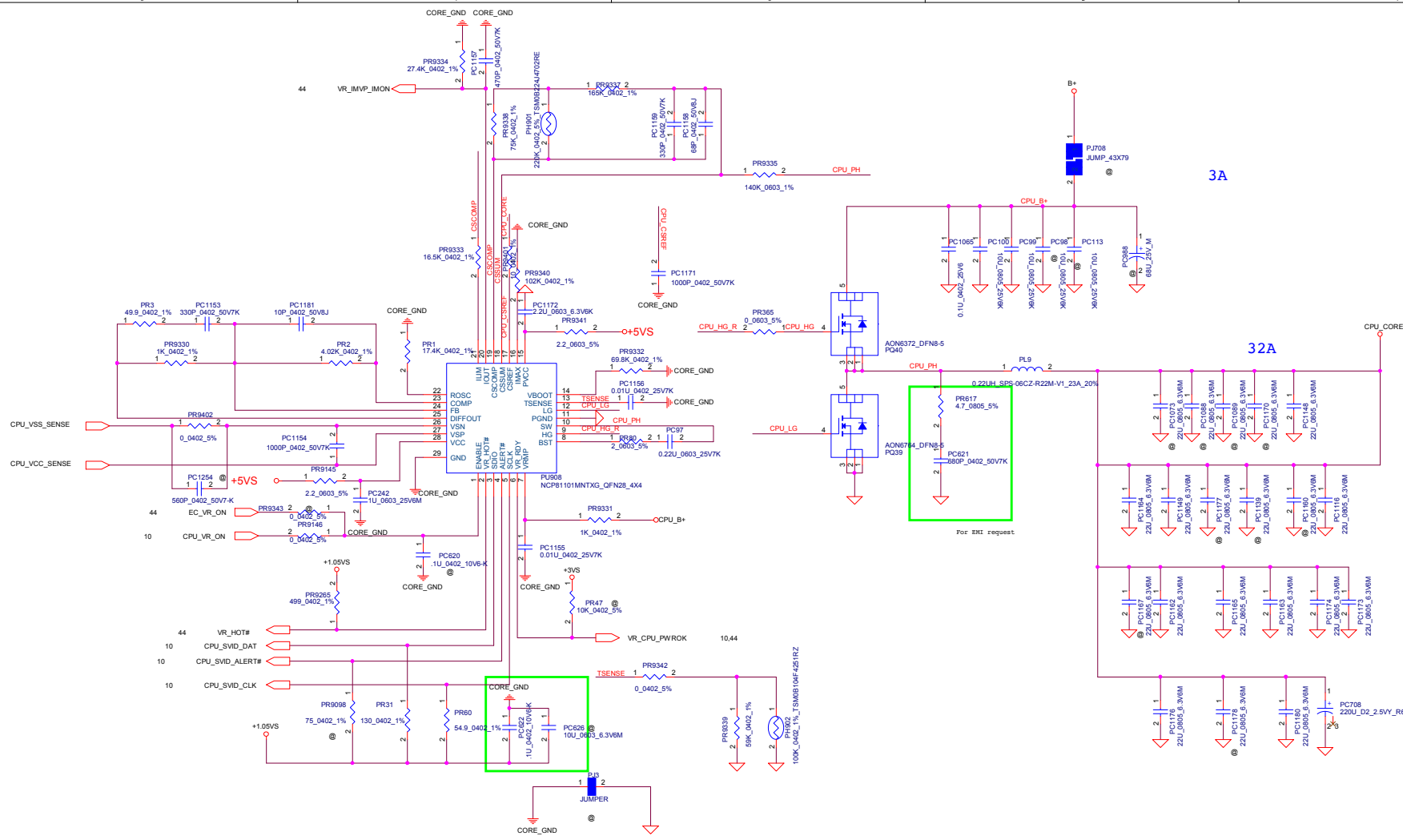




Security Classification		LC Future Center Secret Data		Title	
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